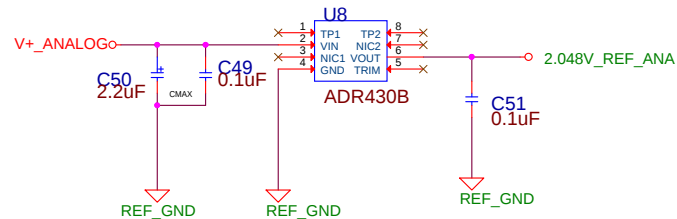
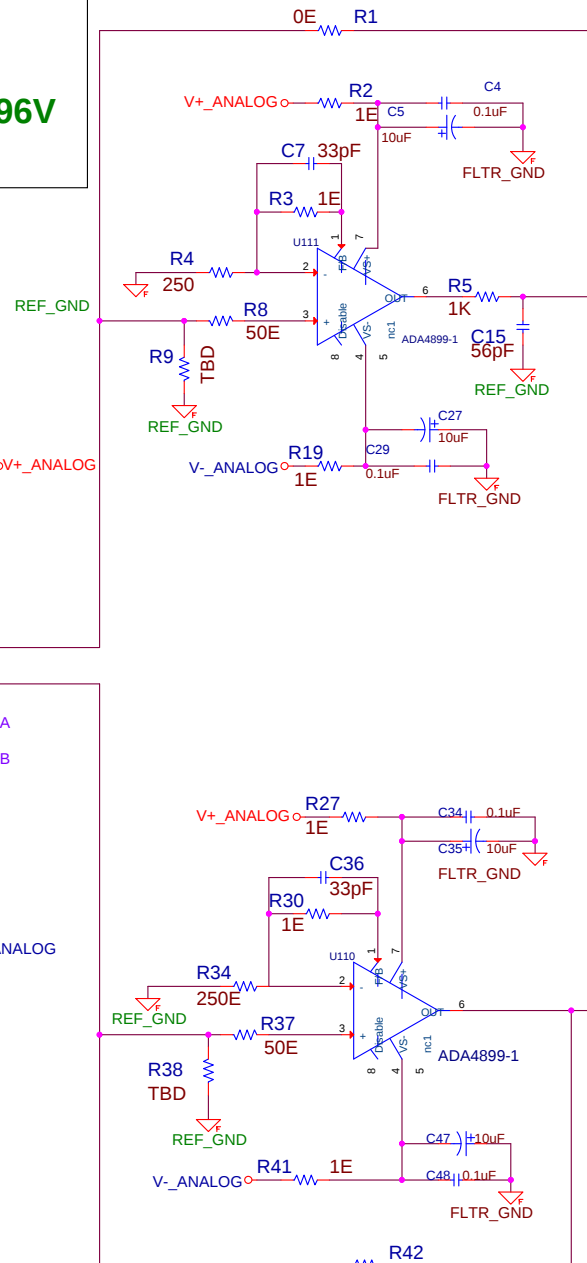


DAC Internal Gain : 2
DAC Power Supply : +/- 5.5V
DAC O/P Volatge Swing : +/- 4.096V
Ref Reg : ADR430B



Offset Amp Gain : 3
Offset Amp. Power Supply : +/- 5.5V
Offset Amp O/P Volatge Swing : 1.01

Assemble 0E and do not assemble Op-Amp to bypass this stage.



Assemble 0E and do not assemble Op-Amp to bypass this stage.

The schematic illustrates a 24-bit sigma-delta ADC system. Key components and their connections are as follows:

- U1: ADG1636** (Multiplexer) selects between **Filter_Restore_CH1** and **V+_ANALOG** for the ADC input. It is powered by **V+_ANALOG** and **V-_ANALOG**.
- U4: ADA4938-V1** (Op-Amp) provides pre-amplification. It is configured with feedback resistors **R12, R13, R17, R21, R22, R23** and is powered by **V+_ANALOG** and **V-_ANALOG**.
- U7: AD8031a/AD** (Op-Amp) provides differential signaling. It is configured with feedback resistors **R31, R32, R33, R34, R35, R36** and is powered by **V+_ANALOG** and **V-_ANALOG**.
- U2: AD7626** (ADC Core) is configured for 24-bit resolution and 100MHz operation. It is powered by **V+_ANALOG** and **V-_ANALOG**. The output is a 24-bit digital signal (**D[23:0]**) and a 100MHz clock signal (**CLK+/-_CH1_4**).
- U9: REG102** (Voltage Regulator) provides a 2.5V supply (**2.5V_VDD2_CH1**) from a 5V input. It is powered by **V+_ANALOG** and **V-_ANALOG**.
- U10: LP2985-50DBVTG4** (Voltage Regulator) provides a 5V supply (**5V_VDD1_CH1**) from a 5V input. It is powered by **V+_ANALOG** and **V-_ANALOG**.

The circuit also includes various passive components for filtering and timing, such as capacitors **C1-C46** and resistors **R1-R46**.

Diff. Amp Gain : 1
Diff. Amp. Power Supply : +/- 5.5V
Diff. Amp O/P Volatge Swing : +/- 4.096V