ANALOG PROCESSING - 1

OPAMP ADA4899-1

Offset Amp Gain : 1
Offset Amp. Power Supply : +/- 5.5V
Offset Amp O/P Volatge Swing : +/- 4.096

OFFSET VOLTAGE-1

Assemble 0E and do not assemble Op-Amp to bypass this stage.

Diff. Amp Gain : 1
Diff. Amp. Power Supply : +/- 5.5V
Diff. Amp O/P Volatge Swing : +/- 4.096V

DAC AD5724

DAC Internal Gain : 2
DAC Power Supply : +/- 5.5V
DAC O/P Volatge Swing : +/- 4.096V
Ref Reg : ADR430B

ADC VDD2 REGULATOR

ADC VDD1 REGULATOR

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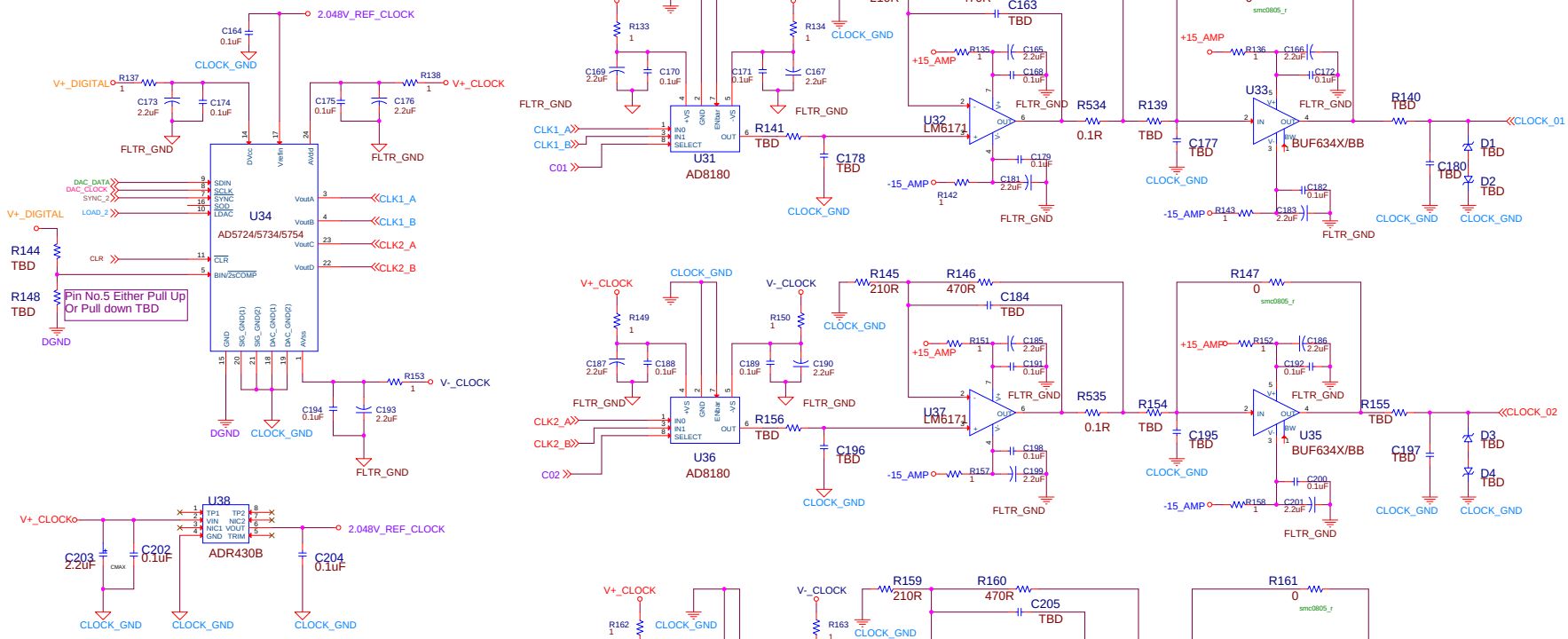
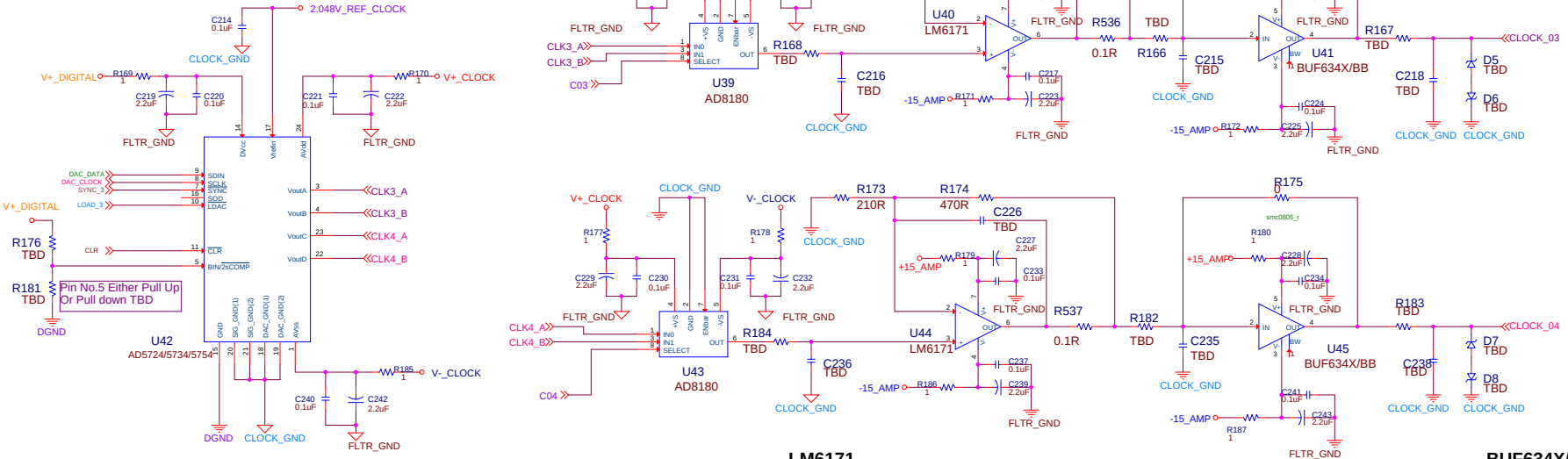
Title: IFPAC
Size: Document Number: D:\KALPESH\CLOCK\TEST_8.DSN Rev: V2
Date: Thursday, January 16, 2014 Sheet 2 of 22

PROGRAMMABLE BILEVEL CLOCK WITH BUF



PROGRAMMABLE BILEVEL CLOCK WITH BUF



DAC 5724 (CLOCK)

DAC Internal Gain : 2
DAC Power Supply : +/- 5.5V
DAC O/P Volatge Swing : +/- 4.096V
Ref Reg : ADR430B
Pin No.5 of DAC : Either BIN or 2's COMP

POWER SUPPLY VOLTAGES

V+_CLOCK: +5V
V-_CLOCK: -5V
+15_AMP: +15V
-15_AMP: -15V

LM6171

Clock Amp. Gain : 3.23
Clock Amp. Power Supply : +/-15V
Clock Amp. O/P Volatge Swing : +/- 13V
Clock OPAMP : LM6171

BUF634X/BB

Gain : 1
Output current : 250mA

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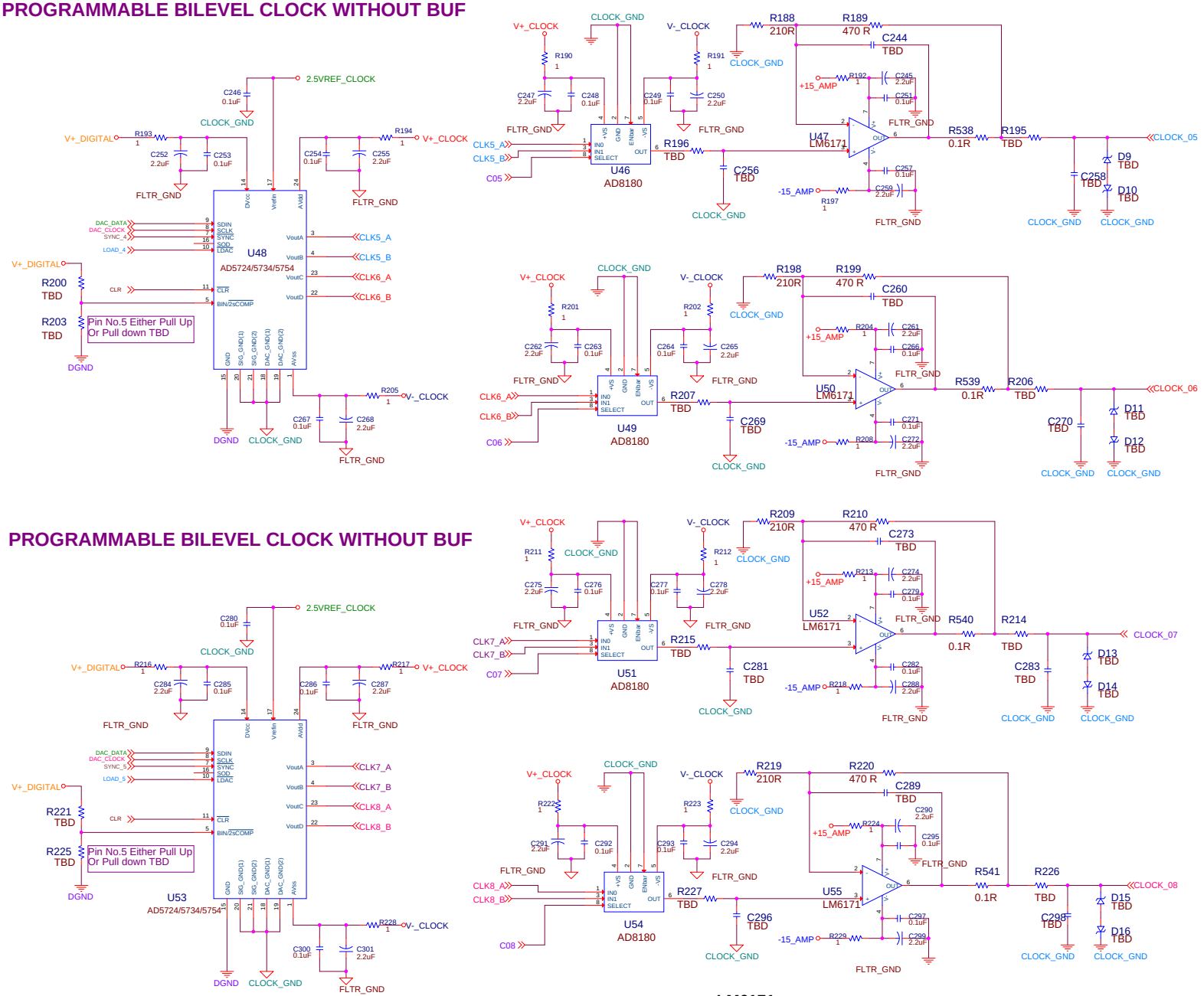
Title: IFPAC

Size: Document Number: D:\KALPESH\CLOCK\TEST_8.DSN — Rev: V2

Date: Thursday, January 16, 2014 — Sheet 6 of 22

PROGRAMMABLE BILEVEL CLOCK WITHOUT BUF



PROGRAMMABLE BILEVEL CLOCK WITHOUT BUF

DAC 5724 (CLOCK)

DAC Internal Gain : 2
DAC Power Supply : +/- 5.5V
DAC O/P Volatge Swing : +/- 4.096V
Ref Reg : ADR430B
Pin No.5 of DAC : Either BIN or 2's COMP

POWER SUPPLY VOLTAGES

V+_CLOCK: +5V
V-_CLOCK: -5V
+15_AMP: +15V
-15_AMP: -15V

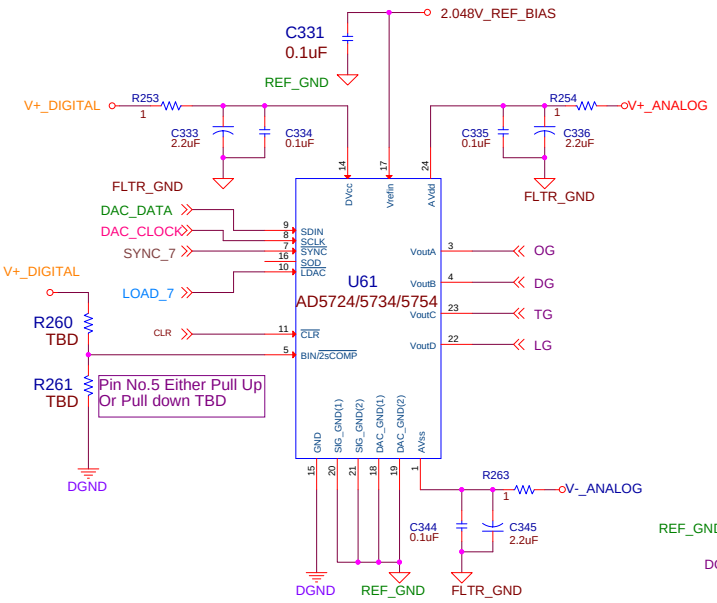
LM6171

Clock Amp. Gain : 3.23
Clock Amp. Power Supply : +/-15V
Clock Amp. O/P Volatge Swing : +/- 13V
Clock OPAMP : LM6171

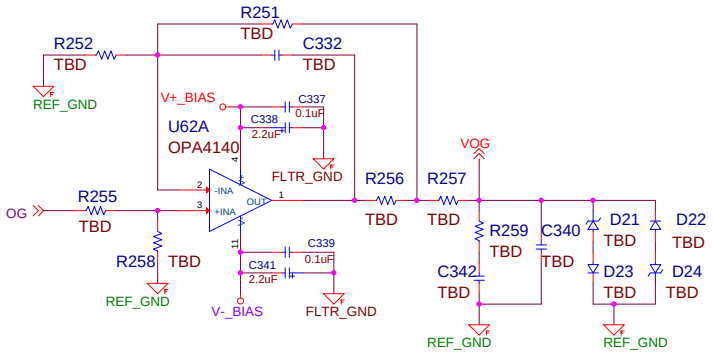
2.048V REF. Regulator is U114
Location :Page Analog_1A

Title	NEW COLD END PCB (V3)	
Size	Document Number	Rev
	C:\Users\rucha\Hawaii\ColdEnd\schematic\loopback_v3.dsn	V3
Date: Thursday, January 16, 2014	Sheet 7 of 22	

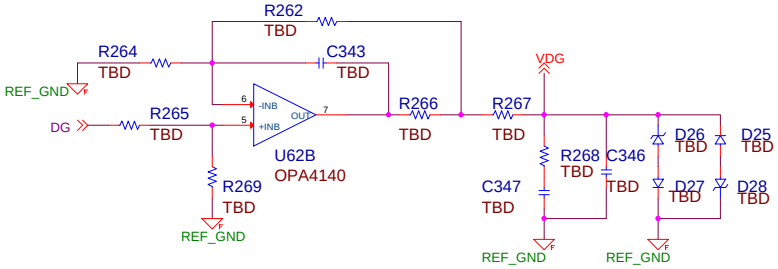
PROGRAMMABLE BIPOLAR BIAS VOLTAGE +/- 17V



GAIN AMPLIFIER OPA4140 = 4.15

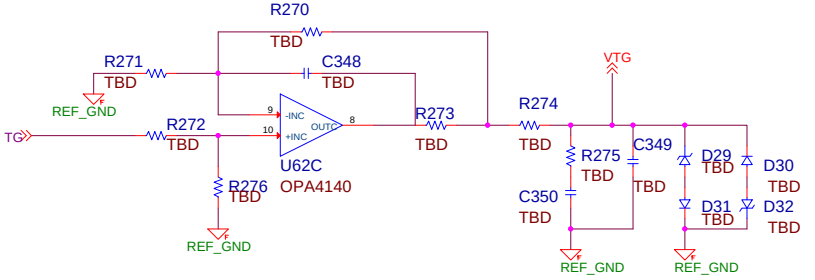


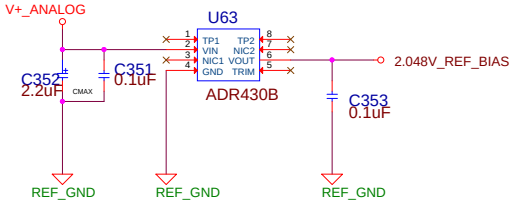
GAIN AMPLIFIER OPA4140 = 4.15



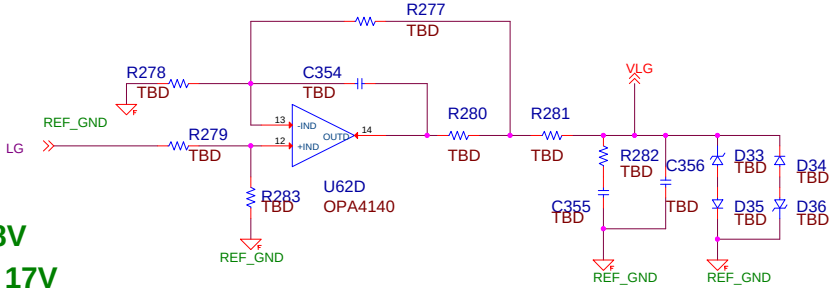
DAC Internal Gain : 2
DAC Power Supply : +/- 5.5V
DAC O/P Volatge Swing : +/- 4.096V
Ref Reg : ADR430B
Ref.Voltage of DAC : 2.048V
Pin No.5 of DAC : Either BIN or 2's COMP

GAIN AMPLIFIER OPA4140 = 4.15





GAIN AMPLIFIER OPA4140 = 4.15

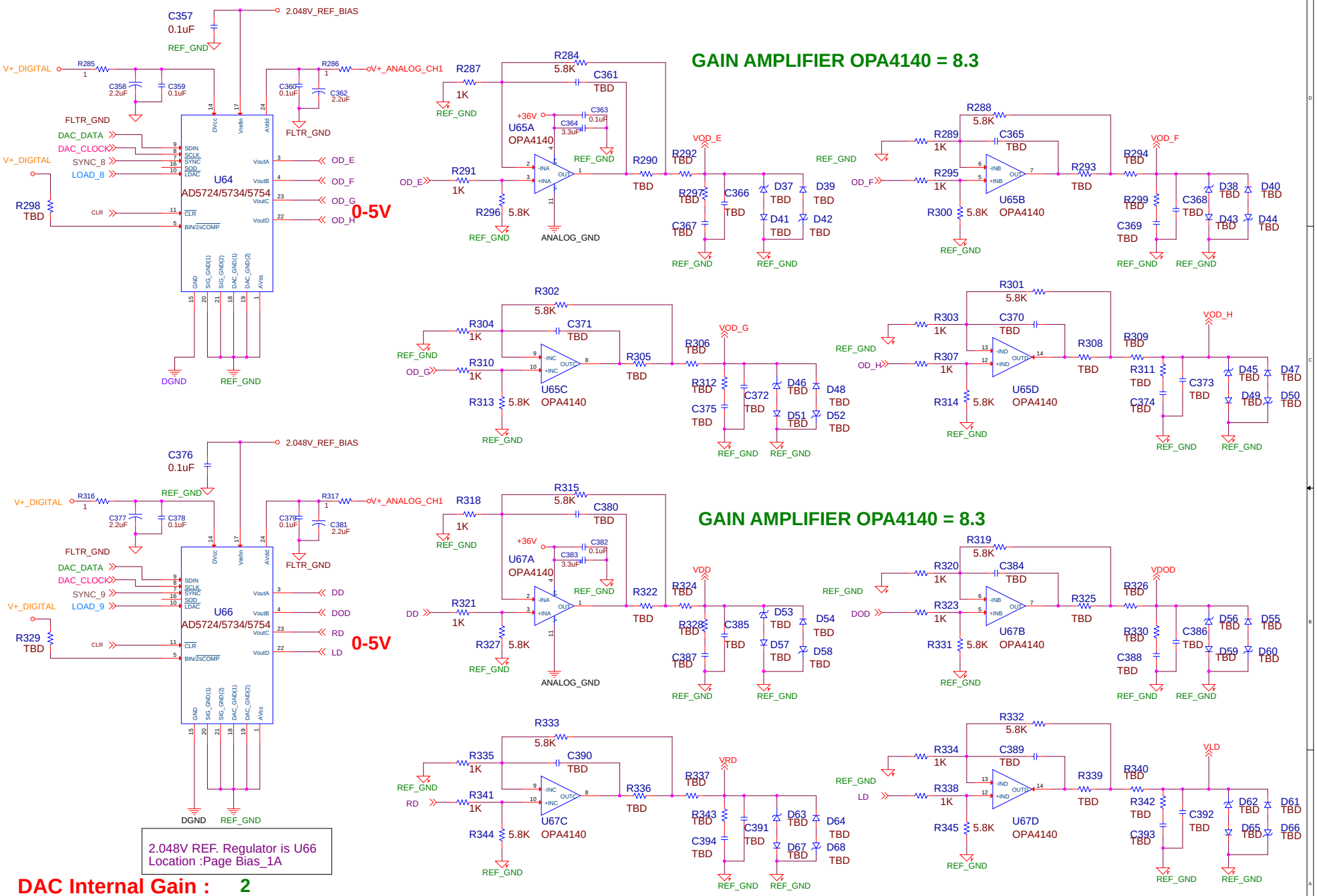


Bias Amp. Gain : 4.15
Bias Amp. Power Supply : +/- 18V
Bias Amp. O/P Volatge Swing : +/- 17V
Bias OPAMP : OPA4140

Title	IUCAA IFPAC
Size	Document Number D:\kalpesh\clock\test_8.dsn — Rev V2
Date:	Thursday, January 16, 2014 — Sheet 9 of 22

PROGRAMMABLE UNIPOLAR BIAS VOLTAGE 0-34V

QTY = 12 No.S (Split in 2 Pages)



2.048V REF. Regulator is U66
Location :Page Bias_1A

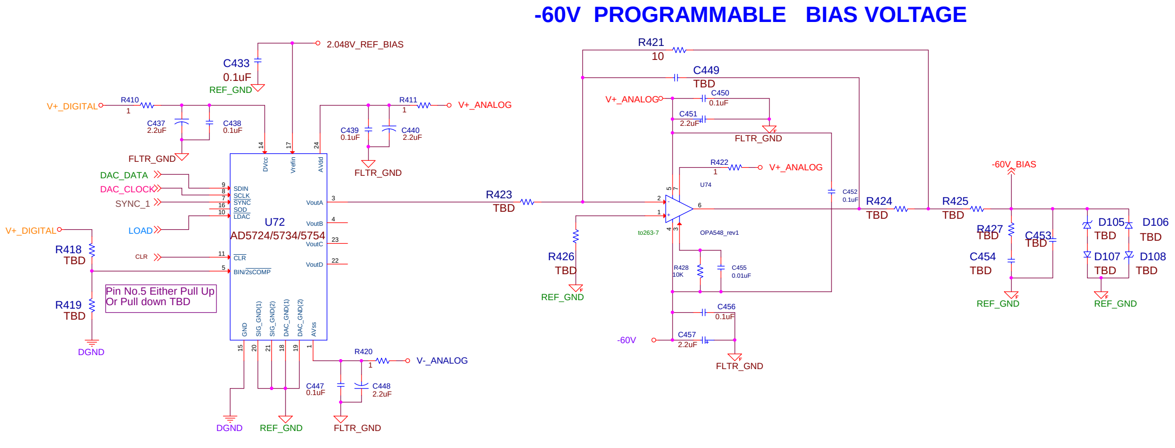
DAC Internal Gain : 2
DAC Power Supply : 5.5V
DAC O/P Volatge Swing : 0 to 4.096V
Ref Reg : ADR430B
Ref.Voltage of DAC : 2.048V
Pin No.5 of DAC : Straight Binary

Bias Amp. Gain : 8.3
Bias Amp. Power Supply : 0 to 36V
Bias Amp. O/P Volatge Swing : 0 to 34V
Bias Opamp OPA4140

2

IUCAA		
Title IFPAC		
Size	Document Number D:\kalpesh\clock\test_8.dsn	Rev V2
Date: Thursday, January 16, 2014	Sheet 10 of 22	

-60V PROGRAMMABLE BIAS VOLTAGE CIRCUIT



2.048V REF. Regulator is U66
Location :Page Bias_1A

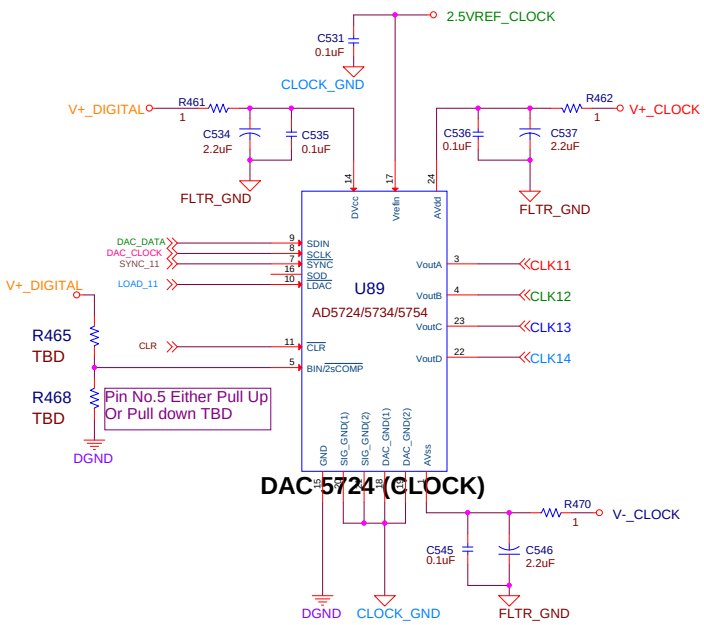
DAC Internal Gain : 2
DAC Power Supply : 5.5V
DAC O/P Volatge Swing : 0 to 4.096V
Ref Reg : ADR430B
Ref.Voltage of DAC : 2.048V
Pin No.5 of DAC : Either BIN or 2's COMP

OPA548 (High-Voltage, High-Current)

Bias Amp. Gain : 15
Bias Amp. Power Supply : +3 V and -57 V
Bias Amp. O/P Volatge Swing : 0 to -55 V
Bias OPAMP : OPA548
High Output Current : 3A Continuous
5A Peak

Title: NEW COLD END PCB (V3)
Size: D | Document Number: D:\kalpesh\vucha\hawaii\ColdEnd\schematic\loopback_v3.dsn | Rev: V3
Date: Thursday, January 16, 2014 | Sheet 12 of 22

PROGRAMMABLE TRILEVEL CLOCK

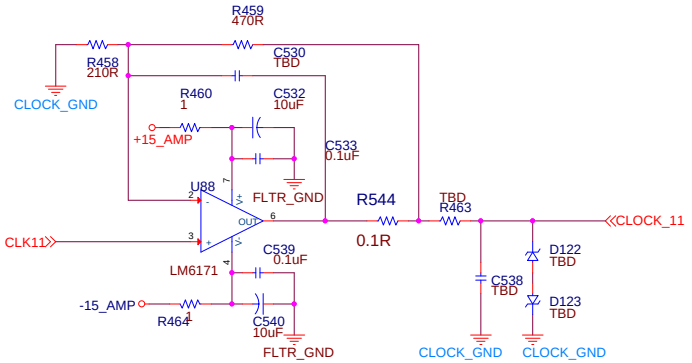


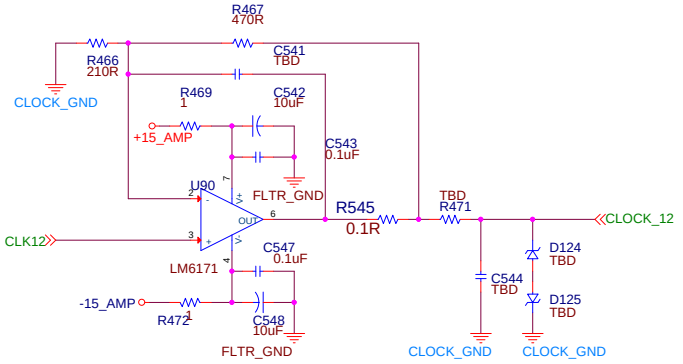
DAC 5724 (CLOCK)

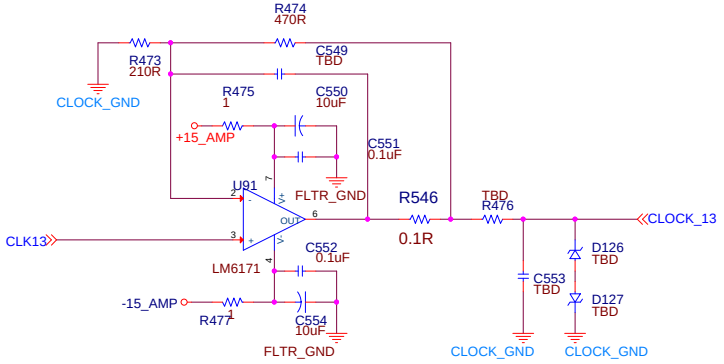
DAC 5724 (CLOCK)

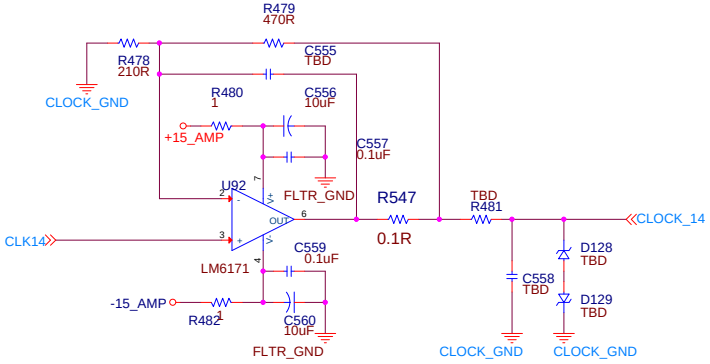
DAC Internal Gain : 2
DAC Power Supply : +/- 5.5V
DAC O/P Volatge Swing : +/- 4.096V
Ref Reg : ADR430B
Pin No.5 of DAC : Either BIN or 2's COMP

Clock Amp. Gain : 3.23
Clock Amp. Power Supply : +/-15V
Clock Amp. O/P Volatge Swing : +/- 13V
Clock OPAMP : LM6171









Title	NEW COLD END PCB (V3)	
Size C	Document Number D:\kalpesh\ruchal\hawaiiColdEnd\schematic\loopback_v3.dsn	Rev V3
Date: Thursday, January 16, 2014	Sheet 18 of 22	