ANALOG PROCESSING

By assembling this resistor (R1) we have option of not using buffer for Offset.

R1 0

OFFSET VOLTAGE-1

V+_ANALOG_CH1 — R2 1 — C5 0.1uF — C6 33pF — R3 499 — U3 AD8099_V3 — R4 250 — R7 50 — R8 50 — R10 50 — C17 2pF — C23 0.5p — C25 10uF CMAX — C26 0.1uF — FLTR_GND_CH1_4

VS3A — VS3B — GND_ANALOG_CH1 — V-_ANALOG_CH1 — R16 1

C20 0.1uF — C21 10uF — C22 0.1uF — R152 1K — C162 56pF

U5 AD5678 — SCLK_TTL — NSYNC_TTL — DIN_TTL — VOUTA — VOUTB — VOUTG — VOUTH — VOUTC — VOUTD — VOUTE — VOUTF — VDD — VREFI/O — GND

DAC C,D,E,F 12 BIT
DAC A,B,G,H 16 BIT

R151 1K — C161 56pF

C30 33pF — R23 499 — U6 AD8099_V3 — R25 250 — R30 TBD — R29 50 — R32 50 — C38 2pF — C39 5pF — VS1A — VS1B

R34 0

By assembling this resistor (R35) we have option of not using buffer for Offset.

OFFSET VOLTAGE-2

U1 ADG1636 — EN — IN1 — IN2 — D1 — D2 — S1A — S1B — S2A — S2B — NC1 — NC2 — NC3 — NC4 — GND — VSS — VDD

Filter Restore — V+_SW_CH1 — V-_SW_CH1 — GND_SW_CH1_4 — C10 10uF — C8 0.1uF — C9 0.1uF — C12 10uF — FLTR_GND_CH1_4

V-_ANALOG_CH1 — R9 1 — C16 0.1uF — C18 10uF — R11 2K — R12 2K — R14 2K — R17 2K — R19 2K — R20 2K

PreAmp+ — PreAmp- — U4 ADA4938_V1 — R15 20 — R18 20 — C24 56pF — C27 56pF — C29 0.1uF — C31 10uF — R24 1 — V+_ANALOG_CH1

R27 1K — C34 56pF — R28 1K

5V_VDD1_CH1 — 2.5V_VDD2_CH1 — C1 0.1uF — C4 0.1uF — C11 10nF — C13 10uF CMAX — R5 10K — R6 10K — C19 0.1uF

10uF Ceramic low ESR — 10uF Ceramic low ESR — C2 — C3 — The 2.5V supply source should supply this pin first and then be traced to the other VDD2 pins(7,18)

U2 AD7626 — VDD1 — VDD2 — CAP1 — REFIN — EN0 — EN1 — IN- — IN+ — GND — VCM — CNV- — CNV+ — D+ — VIO — DCO- — DCO+ — CLK- — CLK+ — REFC — REFB — REFA — CAP2C — CAP2B — CAP2A — PAD

FERRITE 220R 100MHz L1 — C14 0.1uF — C15 0.1uF — C280.1uF

CLK+_CH1_4 — CLK-_CH1_4 — DCO+_CH1 — DCO-_CH1 — D+_CH1 — D-_CH1 — CNV+_CH1_4 — CNV-_CH1_4

R13 100 — R21 100 — R26 100

U7 AD8031a/AD — R22 1 — C32 0.1uF — C33 10uF — R31 1 — C35 0.1uF — C36 10uF — C37 0.1uF — R33 10K

ADC VDD2 REGULATOR

U8 REG102 — ENABLE — VIN — NR — VOUT — GND — NR_CH1 — C42 0.1uF — C44 0.01uF — C40 10uF — R35 0 — R36 11.3K — R38 11.5K — 2.5V_VDD2_CH1

ADC VDD1 REGULATOR

LP2985-50DBVTG4

U9 LP2985-50DBVTG4 — ENABLE — VIN — NR — VOUT — GND — C41 0.1uF — C45 0.01uF — C43 10uF CMAX — R37 0 — 5V_VDD1_CH1

	IUCAA PUNE UNIVERSITY CAMPUS GANESHKHIND	
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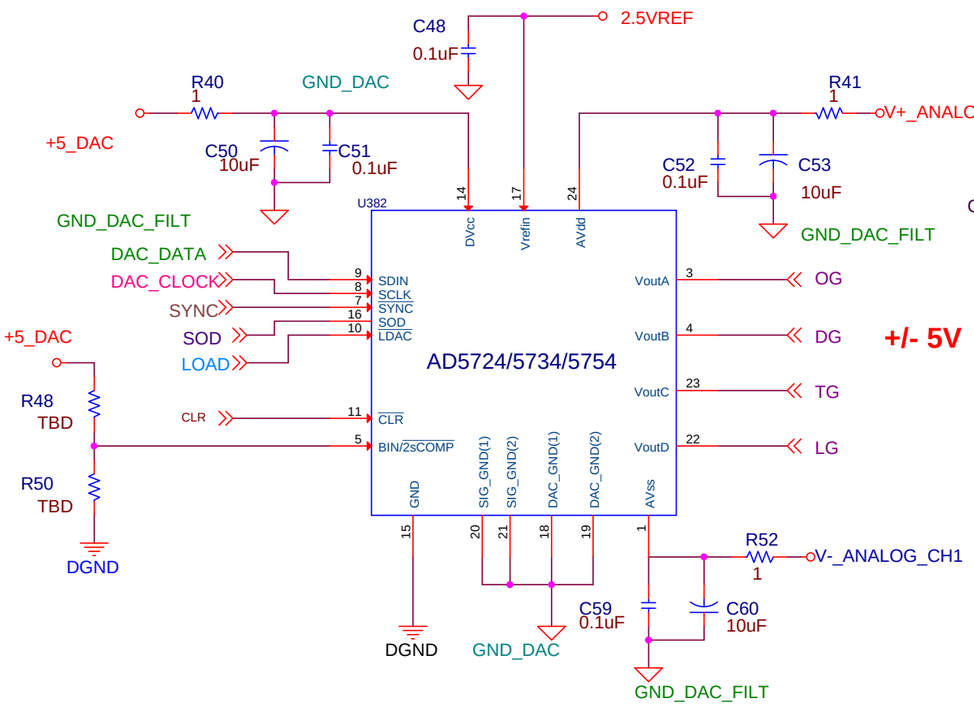
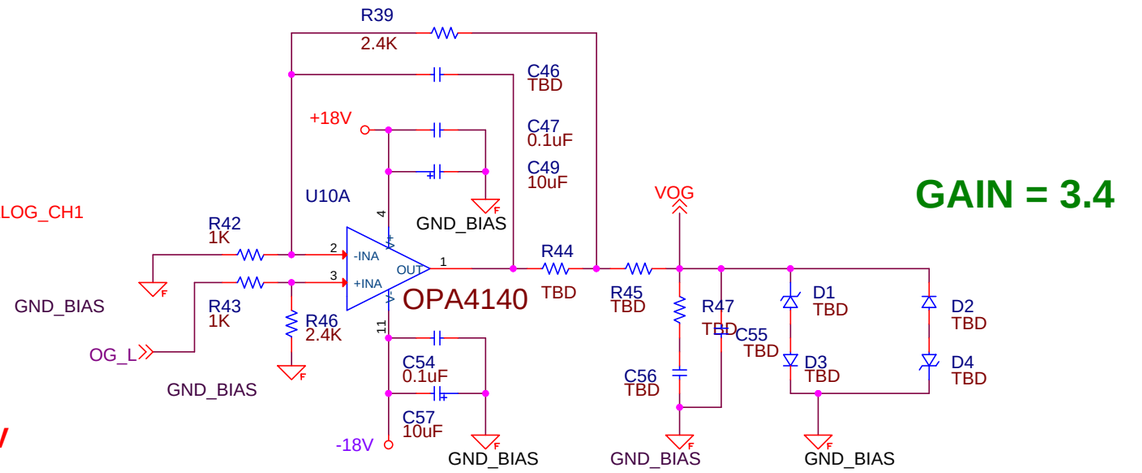
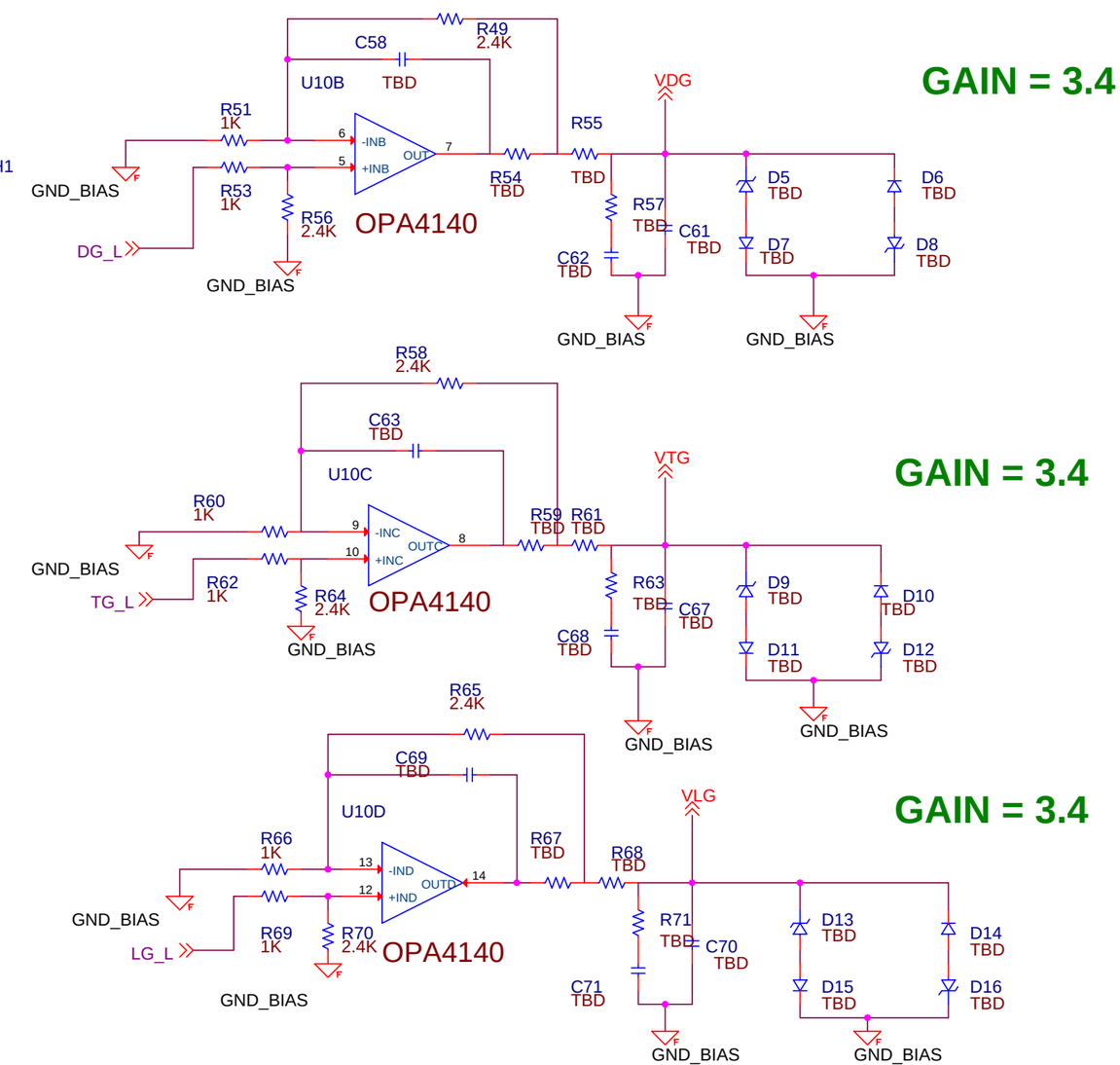
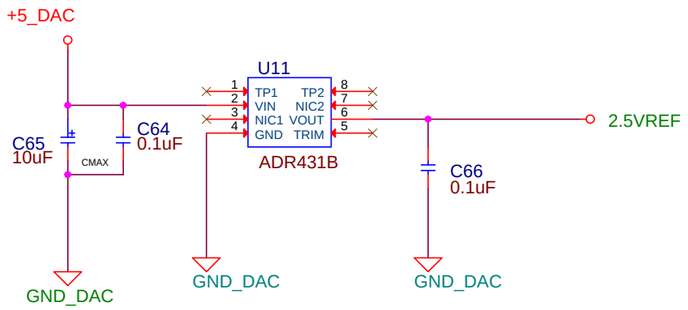
PROGRAMMABLE BIPOLAR BIAS VOLTAGE









V+_ANALOG_CH1 = 5.5V

V-_ANALOG_CH1 = -5.5V

IUCAA		
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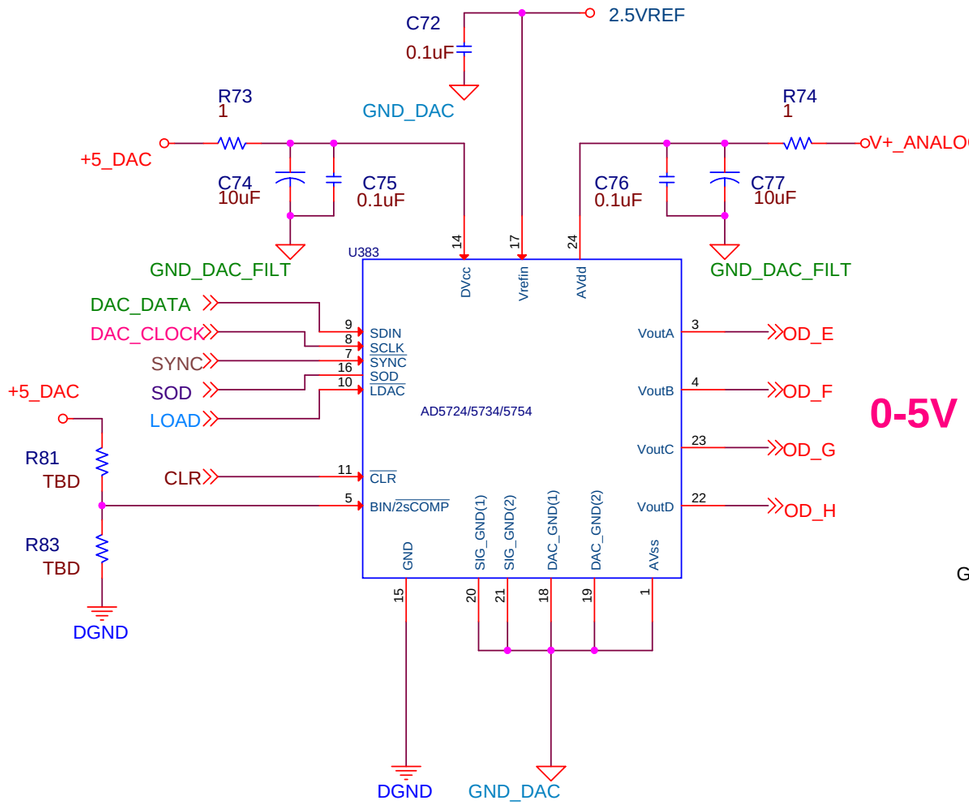
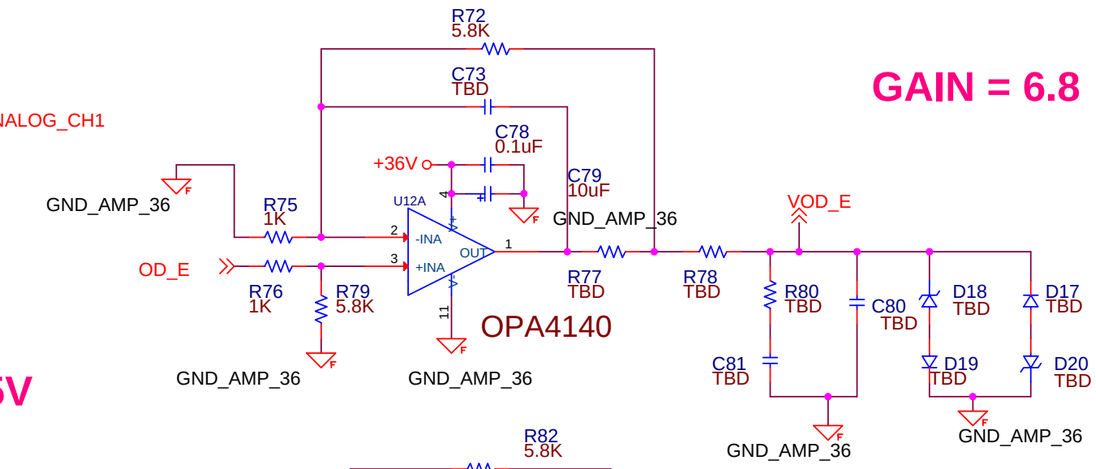
PROGRAMMABLE UNIPOLAR BIAS VOLTAGE



0-5V

V+_ANALOG_CH1 = 5.5V



IUCAA		
Title: IFPAC		
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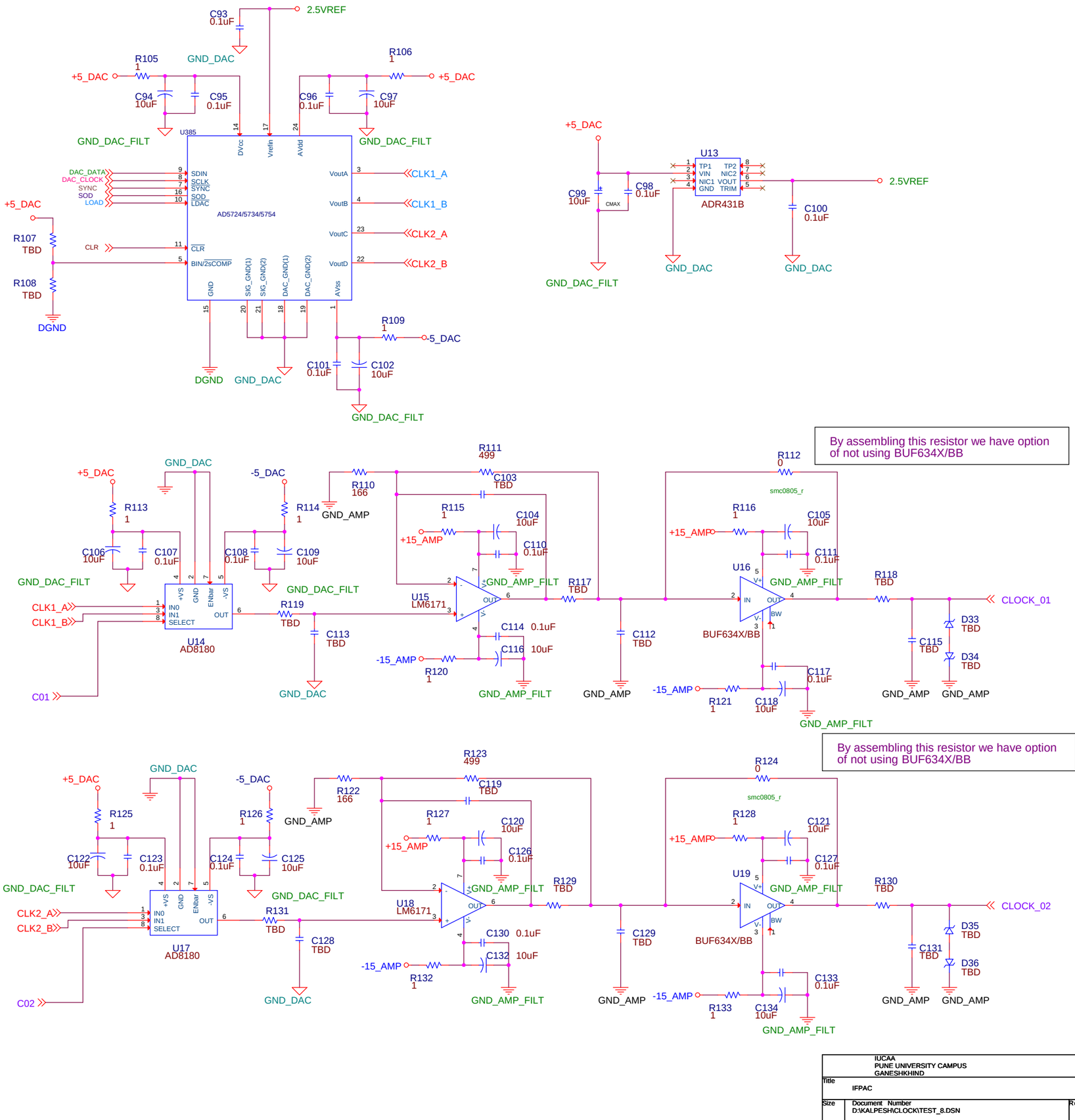
PROGRAMMABLE BILEVEL CLOCK



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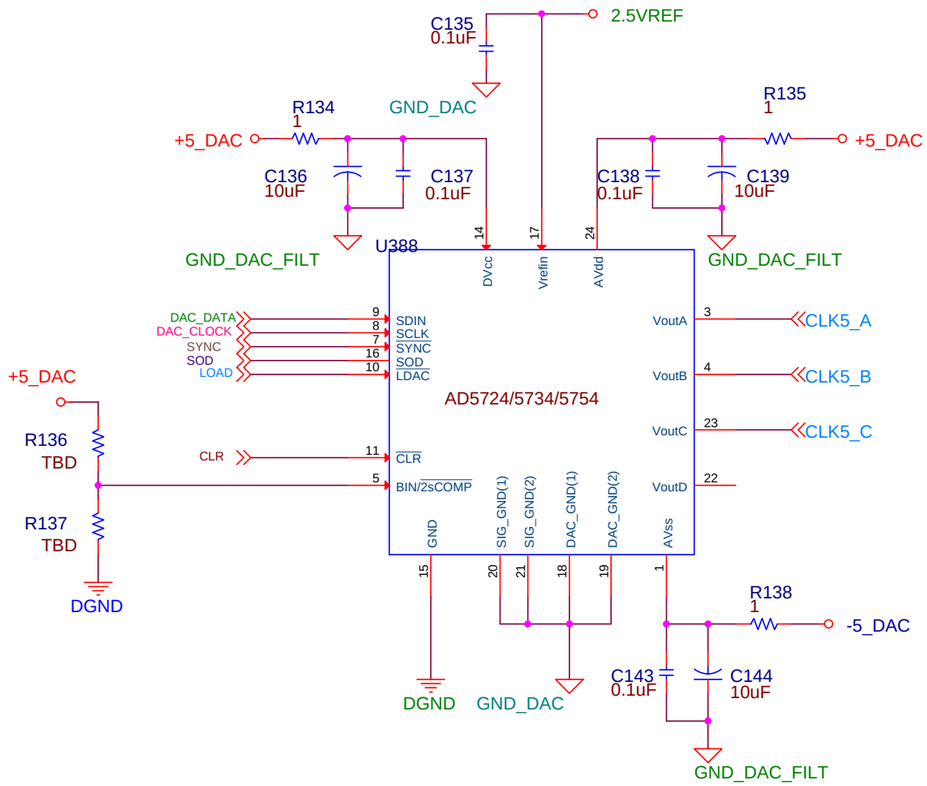
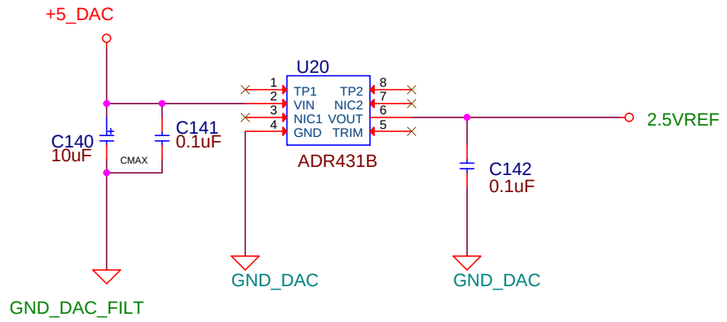
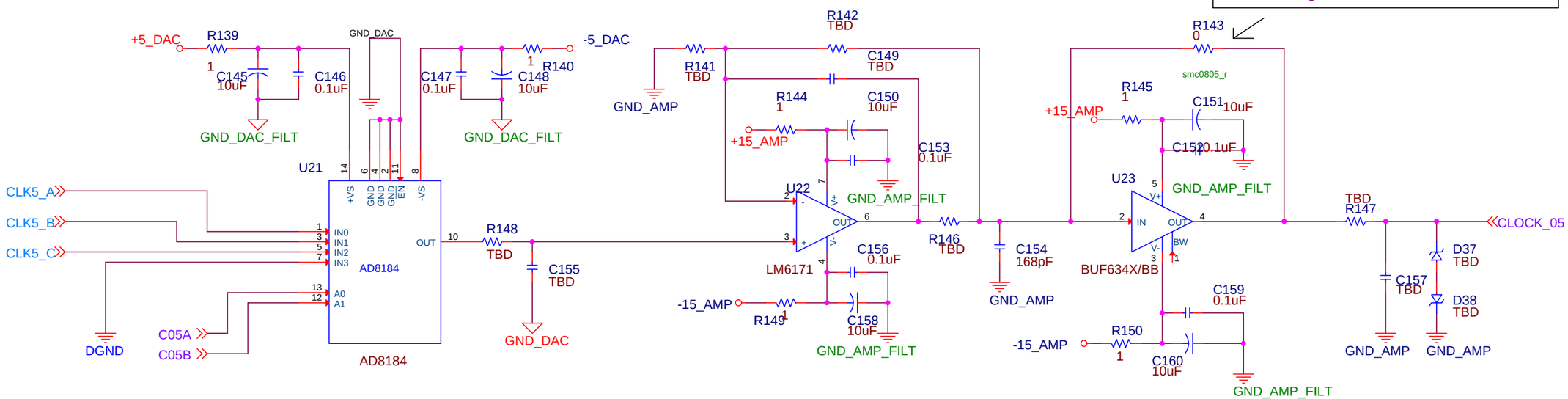
PROGRAMMABLE TRILEVEL CLOCK





By assembling this resistor we have option of not using BUF634X/BB



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