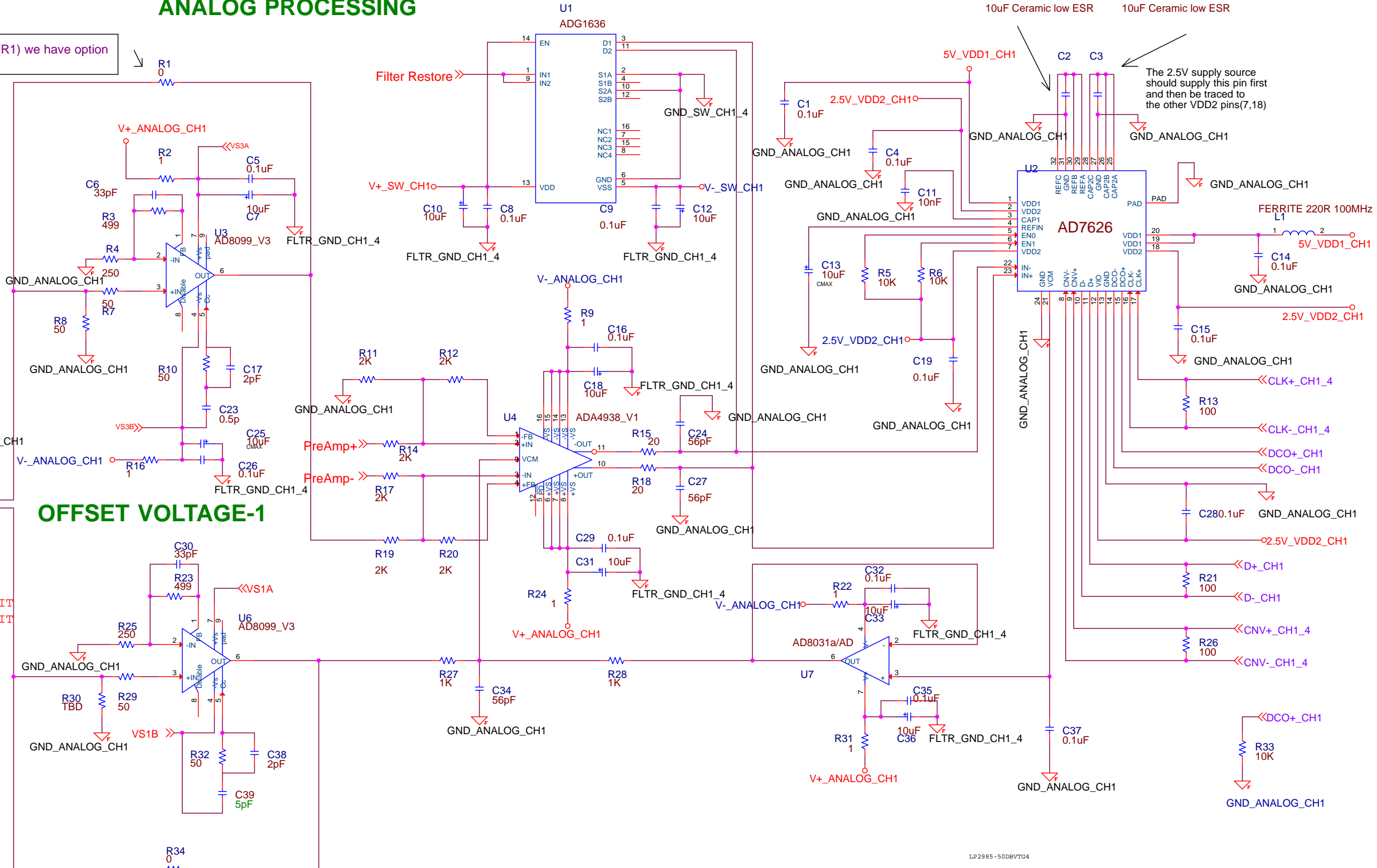


# ANALOG PROCESSING

By assembling this resistor (R1) we have option of not using buffer for Offset.



## OFFSET VOLTAGE-1

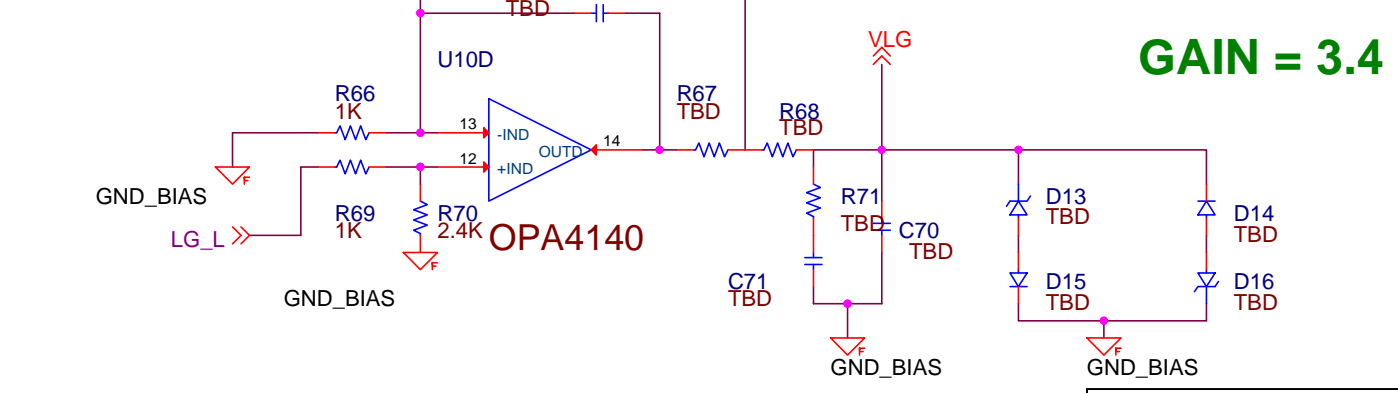
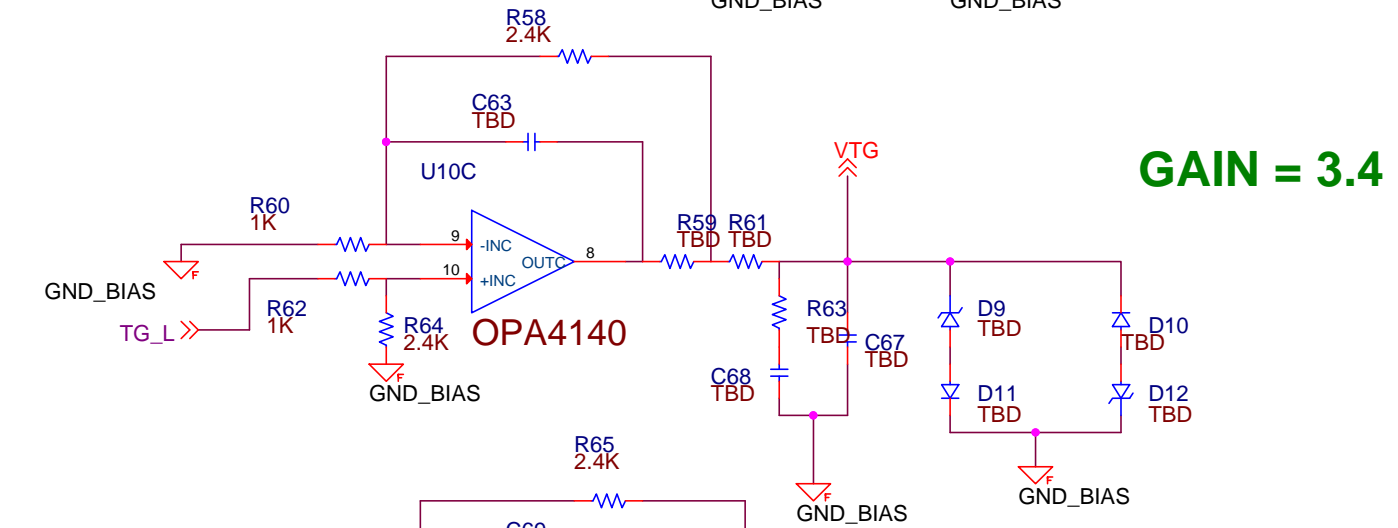
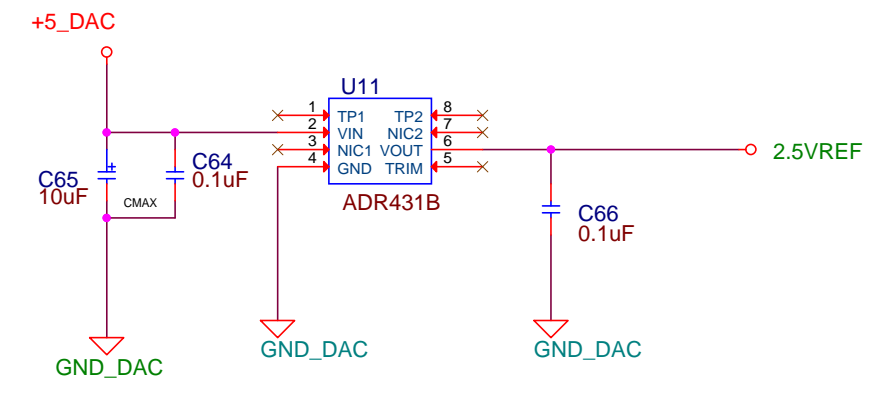
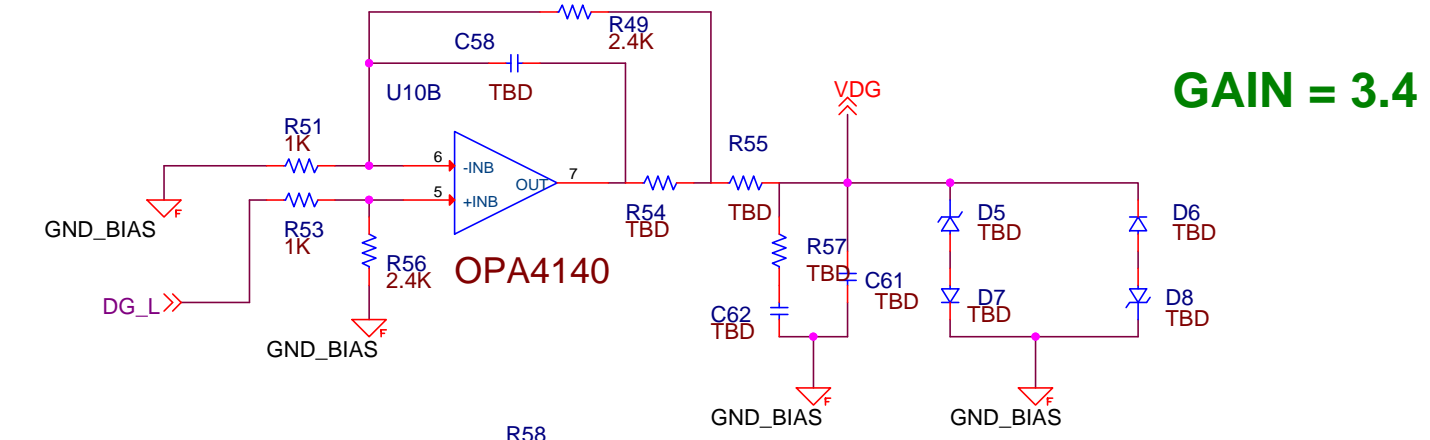
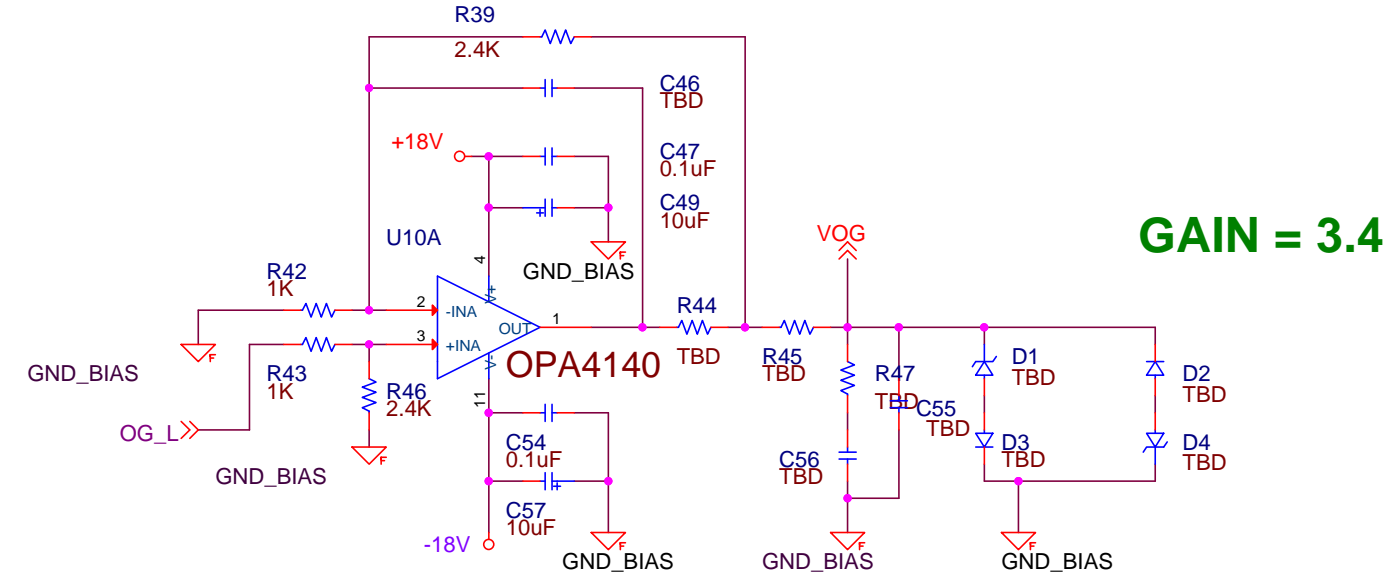
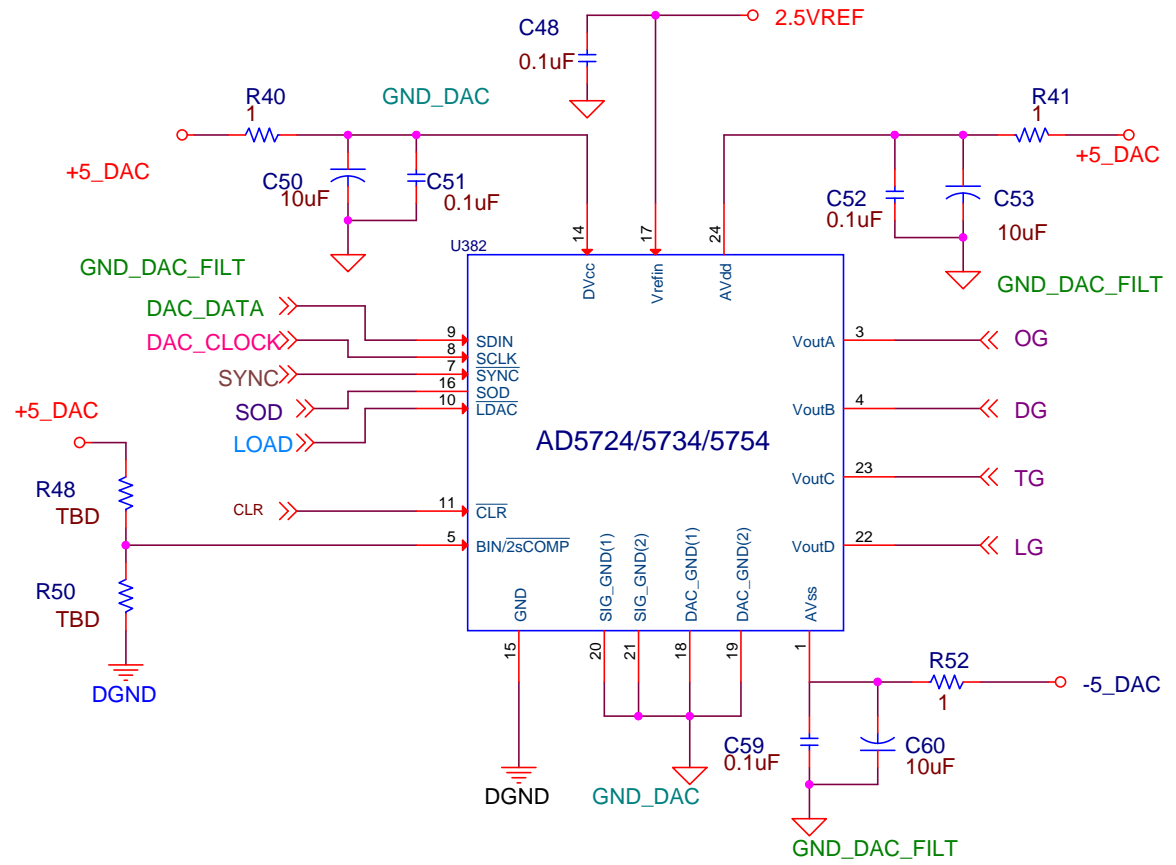
## OFFSET VOLTAGE-2

By assembling this resistor (R35) we have option of not using buffer for Offset.

## ADC VDD2 REGULATOR

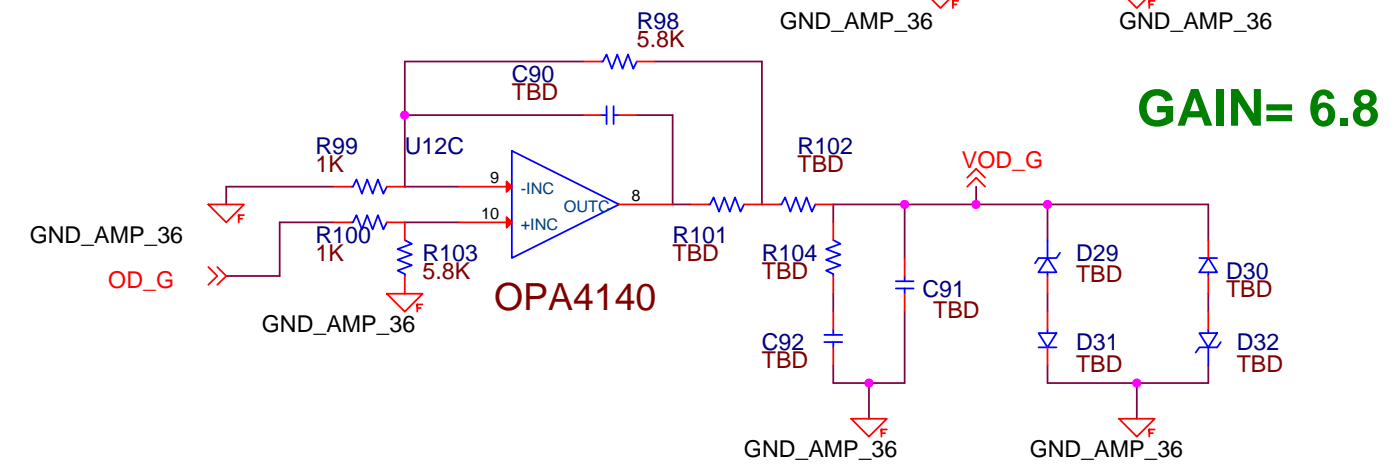
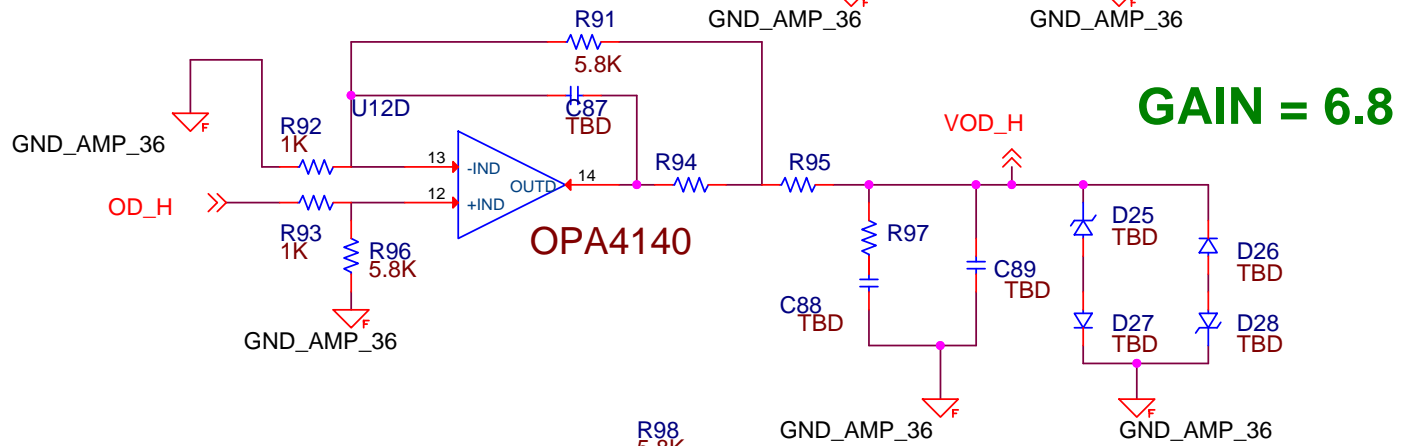
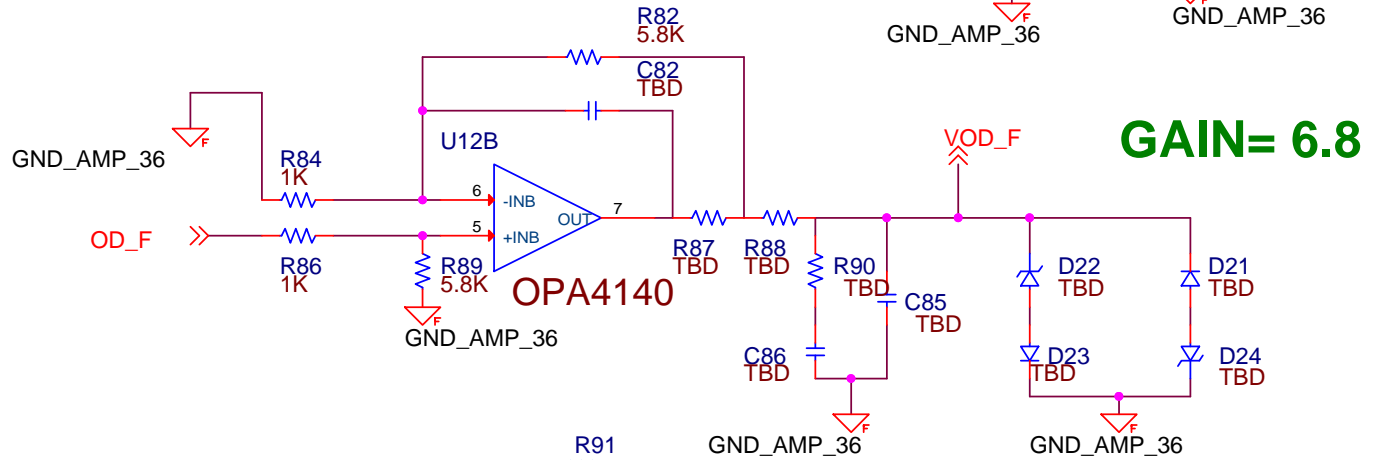
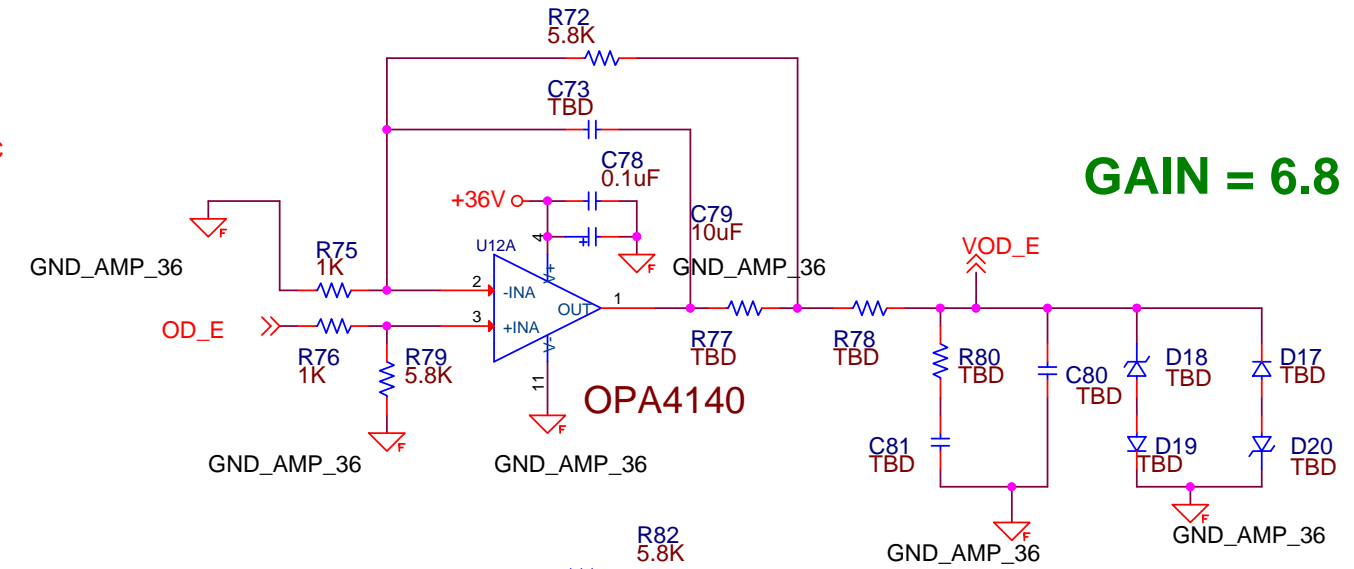
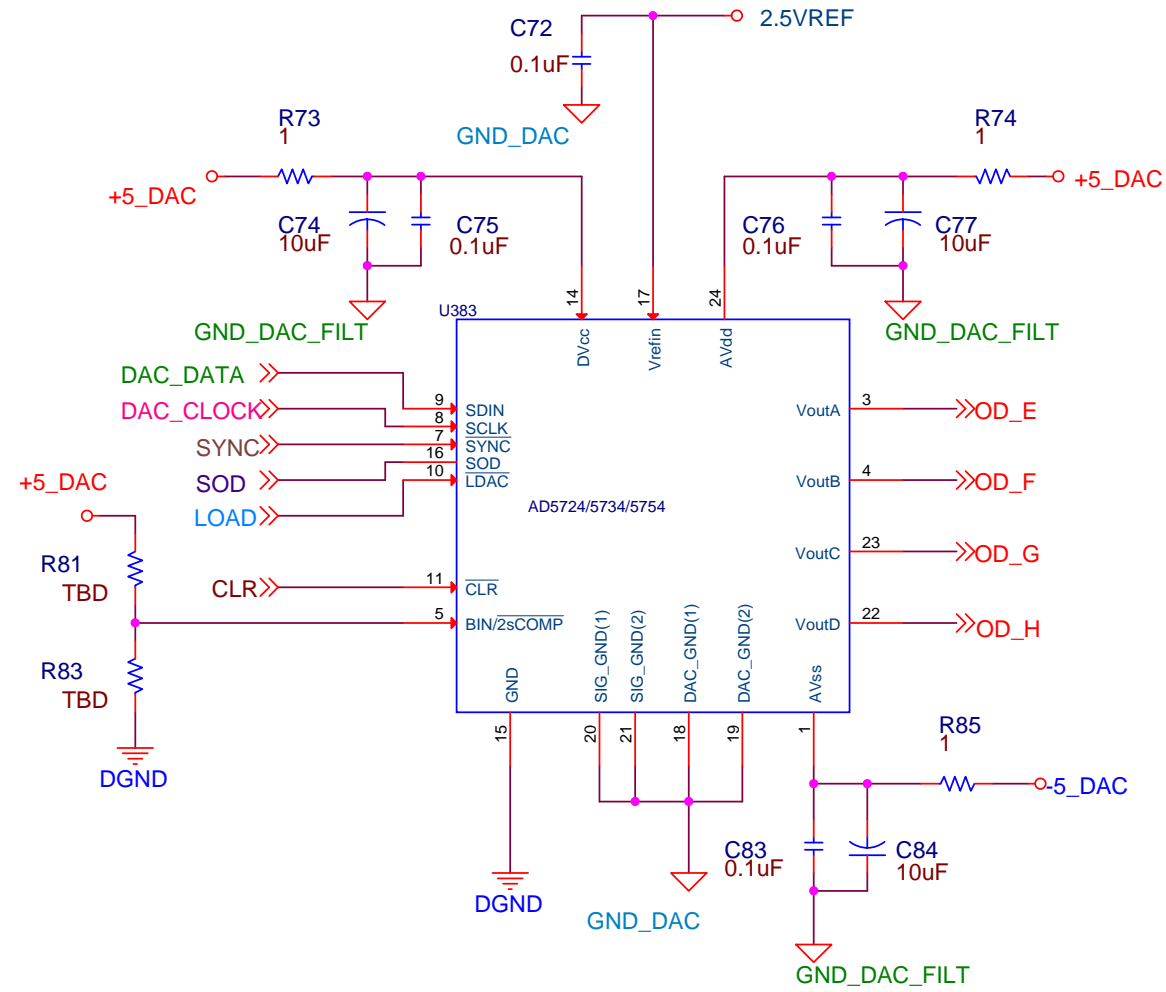
## ADC VDD1 REGULATOR

# PROGRAMMABLE BIPOLAR BIAS VOLTAGE



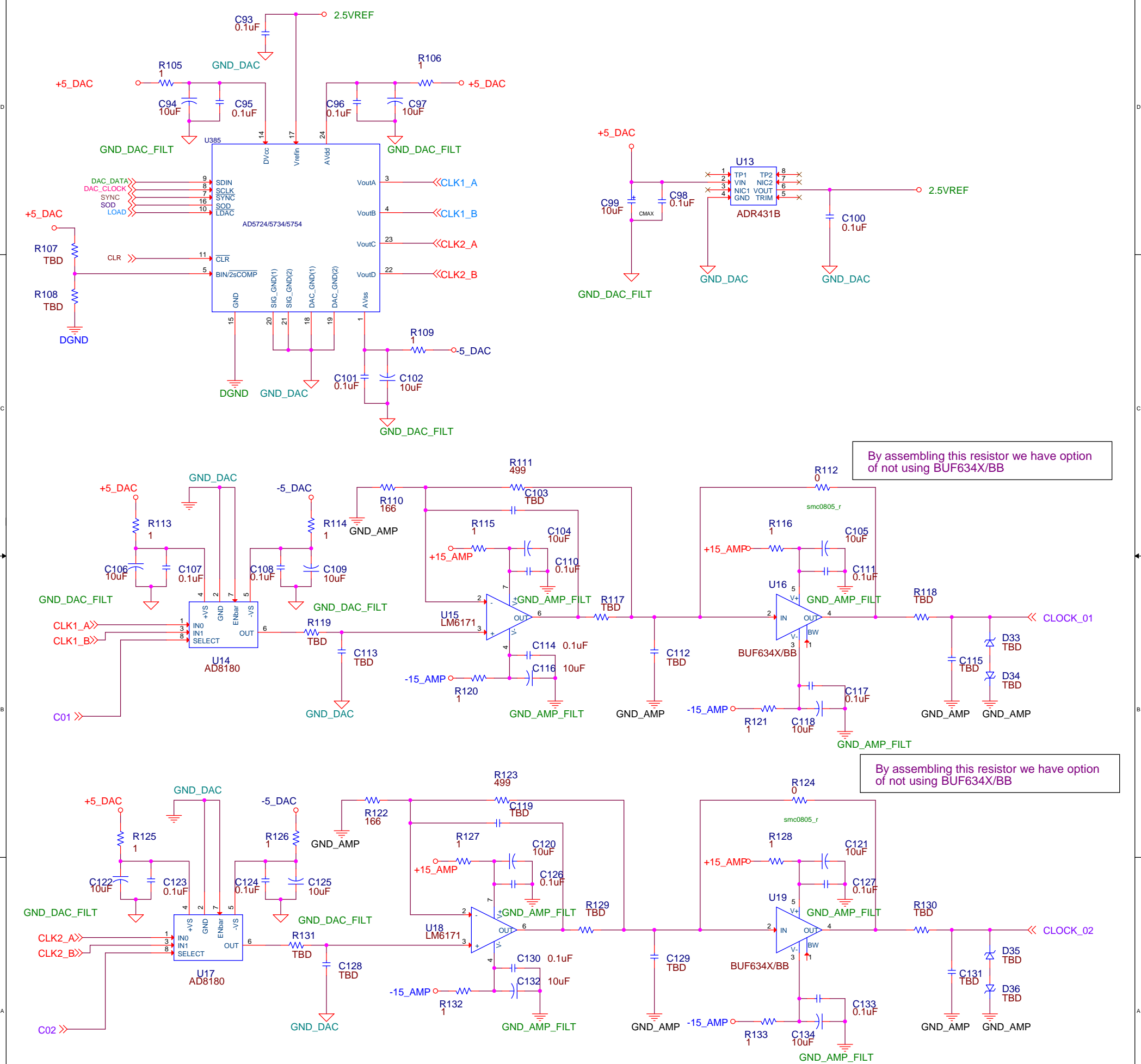
<b>IUCAA</b>		
Title <b>IFPAC</b>		
Size	Document Number D:\kalpesh\clock\test_8.dsn	Rev V2
Date:	Thursday, October 17, 2013	Sheet 2 of 5

# PROGRAMMABLE UNIPOLAR BIAS VOLTAGE

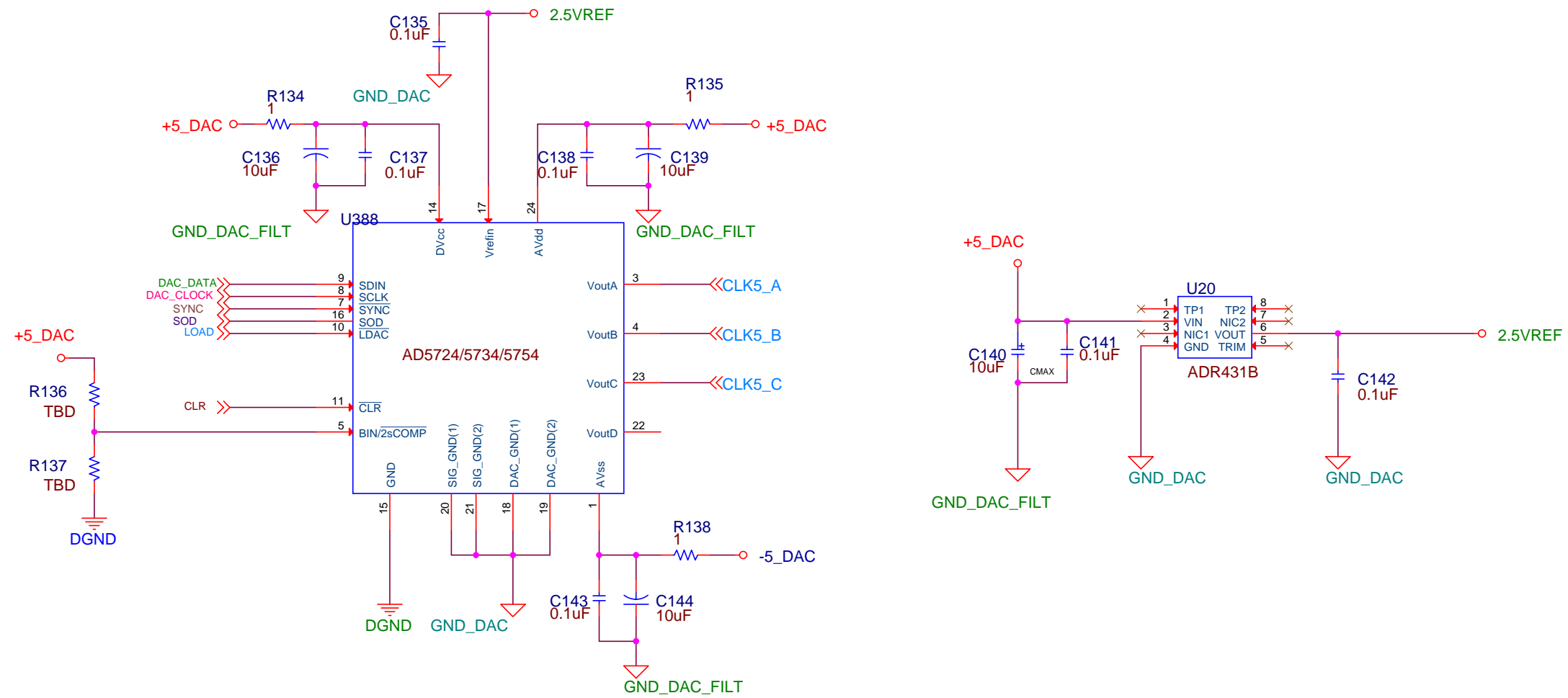


IUCAA		
Title IFPAC		
Size	Document Number	Rev
	D:\kalpesh\clock\test_8.dsn	V2
Date:	Thursday, October 17, 2013	Sheet 3 of 5

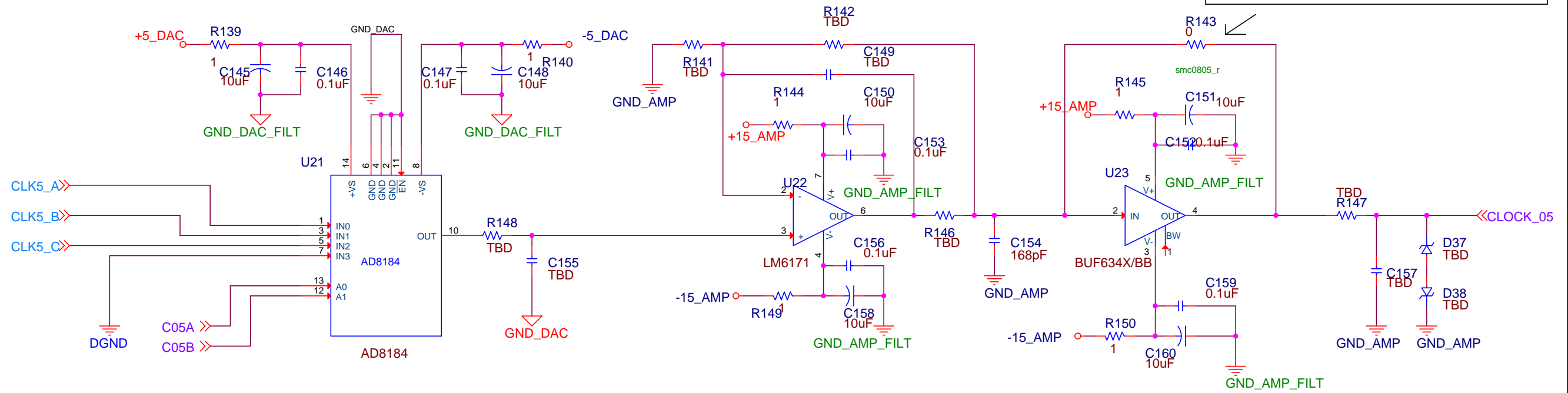
# PROGRAMMABLE BILEVEL CLOCK



# PROGRAMMABLE TRILEVEL CLOCK



By assembling this resistor we have option of not using BUF634X/BB



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Title IFPAC		
Size	Document Number D:\KALPESH\CLOCK\TEST_8.DSN	Rev v2
Date: Thursday, October 17, 2013	Sheet 5 of 5	