Meeting Notes October 17, 2013

Attendees: Stephen Kaye, Pravin Chordia, Mahesh Burse

**Minutes**

* Pravin presented and discussed results from clock driver testing. The tests were to demonstrate the utility of filters placed in the clock driver signal path.
* Some questions remain as to how the component values were selected. The in-loop-compensation topology was defeated by using a 0 ohm resistor for the output isolation resistor.
* Further tests should be done with the clock driver circuit.
* The schematic for the analog signal chain was presented
* The DACs used for the offset voltages need to be investigated as to the noise specifications.
* Buffers for the offset voltages may need some filtering. This will be studied.
* Schematics for the bias voltages was presented
* The amplifier for the bias voltages was changed to an OPA4140.
* The OPA4140 needs to be studied will respect to noise requirements.
* The DAC range for the bias voltages is selectable to be either 0-10V or -5V to +5V. This will require a change in the gain of the bias amplifiers.
* A schematic for tri-level clocks was presented
* A 4x1 analog multiplexer/switch was used to switch between the clock levels. This scheme is different than anticipated. Advantages and disadvantages need to be investigated.
* The waveform definition scheme was discussed
* It was clarified that multiple tables can be called arbitrarily. This indicates that the scheme is more flexible than previously thought.
* Caltech will create desired tables and calling sequences to make sure the scheme is what we want.
* Readiness for the prototype demo in October was discussed. A computer and power supply are needed at Caltech for the test.
* Power rating of supply is still TBD. The computer operating system will be Red Hat Enterprise Linux.
* Information concerning power supply capacity for the test will be sent
* Prototype will be sent by the end of the month

**Action Items**

**IUCAA**

* + Continue clock driver testing. Qualify reasons for component selection.
  + Review DAC for signal chain offsets. Noise specs., range, etc.
  + Supply requirements for power supply for prototype demo
  + Continue readying the prototype for delivery.

**Caltech**

* + Reply with number of parallel (tri-level) clocks needed.
  + Create desired waveforms and the sequence to call the waveform tables