Meeting Notes October 2, 2013

Attendees: Stephen Kaye, Pravin Chordia

**Minutes**

* No new DAC or switch has been found. As of now the switch allows +- 3V and the DAC is 12 bits with a range of +-5V
* Clock driver simulations were discussed. As designed, a load of 680 pF will cause the phase margin to go negative. This will be unstable
* Clock driver with compensation for the capacitive load allows for 50 degrees of phase margin
* A new clock driver amplifier has been found with 130mA of drive current.
* A more flexible waveform generator is desired. The science CCDs won’t always follow the readout sequence of state tables. Flexibility is desired for unforeseen modes of charge shifting.
* Hardware for the prototype demo are packaged. Some software work still needs to be done. Demo will be shipped in about two weeks.

**Action Items**

**IUCAA**

* + New clock driver amplifier will be tested
  + Do SPICE simulation of clock driver circuit
  + Review latest controller definition document

**Caltech**

* + Double check controller document posted to twiki. The comments are turned on.
  + Email comments on waveform generation document