Meeting Notes September 19, 2013

Attendees: Stephen Kaye, Pravin Chordia, Mahesh Burse

**Minutes**

* Discussed waveform sequence document
* User constructs waveform tables. They can be 512 clock states each.
* User sends information concerning size of CCD, readout area, overscan, dark pixels, etc. and FPGA creates the sequence of the tables to perform the correct read out.
* Mapping of clocks, shutter signals, and ROI sections still need to be read
* Sharing of schematic capture files was attempted, but not successful
* IUCAA using v16.6 OrCad. Altium may not be able to import this format.
* Search for fast mux which covers +-5V range was unsuccessful. +-5V muxes are too slow.
* Searching now for a different DAC which will stay within mux voltage output range.
* Work on prototype demo continues. Software is being programmed, and an enclosure for the cards is being made.

**Action Items**

**IUCAA**

* + Send v16.2 OrCad schematic of clock driver
	+ Do SPICE simulation of clock driver circuit
	+ Review latest controller definition document

 **Caltech**

* + Review LM6171 datasheets and email more questions about clock driver circuit
	+ Read and digest the last part of IUCAA’s waveform generation scheme
	+ Do SPICE simulation of clock driver circuit
	+ Contact Altium about importing OrCad files