Meeting Notes Setember 4, 2013

Attendees: Stephen Kaye, Roger Smith, Pravin Chordia, Mahesh Burse

**Minutes**

* Discussed the controller definition document
* Power supply design will be deferred until bias and clock design is done. Appropriate power supplies will be chosen based on PSRR and other bias and clock filtering
* Substrate driver current capability needs to be determined
* A new voltage biasing scheme for the higher bias voltages was introduced. The concept needs to be developed and will be drawn up
* We are converging on a final document quickly
* Steve will merge the comments into the text and send out a final draft
* Pravin will have a clock driver circuit by next telecon
* Discussed circuit simulation
* We will be using simulation and trade netlists of circuit sections

**Action Items**

**IUCAA**

* + Identify appropriate 12 bit DAC for design
  + Complete new clock driver design – share netlist
  + Continue work on prototype demo in October

**Caltech**

* + Get data sheet for focus/guider CCD to Pravin
  + Determine substrate driver current specification
  + Draw up voltage biasing scheme for higher bias voltages
  + Merge comments into text of controller definition document
  + Test exporting and importing netlists into simulation software
  + Send links to IUCAA for MultiSim and Altium