ZTF CCD Controller

Architecture and Performance Requirements

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August 14, 2013

# Purpose of this document

The purpose of this document is to guide the development of the version of IFPAC, which will control the WaSP and ZTF CCDs. The architecture, capabilities, performance requirements for hardware and software components will be defined and constraints on space and power, etc will be discussed. It is anticipated that this document will serve as an early version of a full design description, and will thus read as such but the initial intent is to develop a consensus on the goals of the development project.

# Division of responsibility

**COO:**

* VIB including preamps.
* Cables.
* Chassis
* Temperature monitoring and control.

**IUCAA:**

* Single Board Controllers.
* Programmable timing generator (FPGA coding)
* DCDS processing (FPGA coding)
* Diagnostic capabilities.
* Data links and host interface.
* Host API
* Data buffering and FITS writer

**TBD:**

* Modular power supply (plug in); power line filtering, power switch, front panel LED power control.
* Waveform development software (prepare definitions, plotting).
* Host software for diagnostics.
* Backplane development

COO is asking IUCAA to provide subsystems that can be configurable by COO, and not a turn-key system with predetermined modes of operation. Modes of operation are being discussed in the interests of an open discussion of likely use cases and not with the intent of having these modes programmed into the controller by IUCAA. The design must be modular and flexible enough to be reconfigured as required and COO must have confidence in its ability to use these tools to do so. The best way to assure this is to have COO configure the system for the specific CCDs and readout modes using the tools supplied by IUCAA.

# Application to WaSP

WaSP is a wide field imager at the Hale 200” prime focus which consists of one wafer scale 6K\*6K 15µm pixel CCD (e2v CCD231-C6) read through 4 true differential outputs. A on one edge of the field there is a close butted guide and focus CCDs, both 2K\*2K 15µm STA CCDs delta doped and packaged by JPL.

The STA CCDs will use the output amplifiers at each end of a serial register to form a differential pair feeding one video chain so that two outputs can be read out simultaneously. The polarity of the signal will be reversed if the serial clocking direction is reversed. We will supply a way to accommodate this in the video chain by applying a full-scale output offset which will, in effect, cause a signal inversion for the reverse readout direction.

# Application to ZTF

A mosaic of 16 e2v CCD231-C6 CCDs will be read through 4 channels each at 1Mpixels/s/ch. One guide and 3 focus CCDs placed in the chords of the field of view will be read through 2 channels each.

# ZTF System Layout

The mosaic of CCDs is operated by a set of single board CCD controllers, each of which serves 4 video channels. All single board controllers use the same master clock and are synchronized by a single frame start pulse, which can be generated by any of them. (The frame start is an open collector output driving a bus line, which all controllers listen to.) Since all controllers execute exactly the same readout algorithm, they will remain in sync.

AC couplers and differential video preamps are located inside the dewar close to the CCDs on the Vacuum Interface Board (VIB). In the case of WaSP the single board controllers plug directly into the VIB while for ZTF commercial cables carry signals to controller boards located outside the telescope tube.

One data link per controller board connects back to a collection of host processors each storing images on its local disk. The number of single board controllers per host computer is to be determined by link data rate capability. The data system topology is shown below in Figure 1 and is discussed later in Host Computers and Data Handling section on page 40.

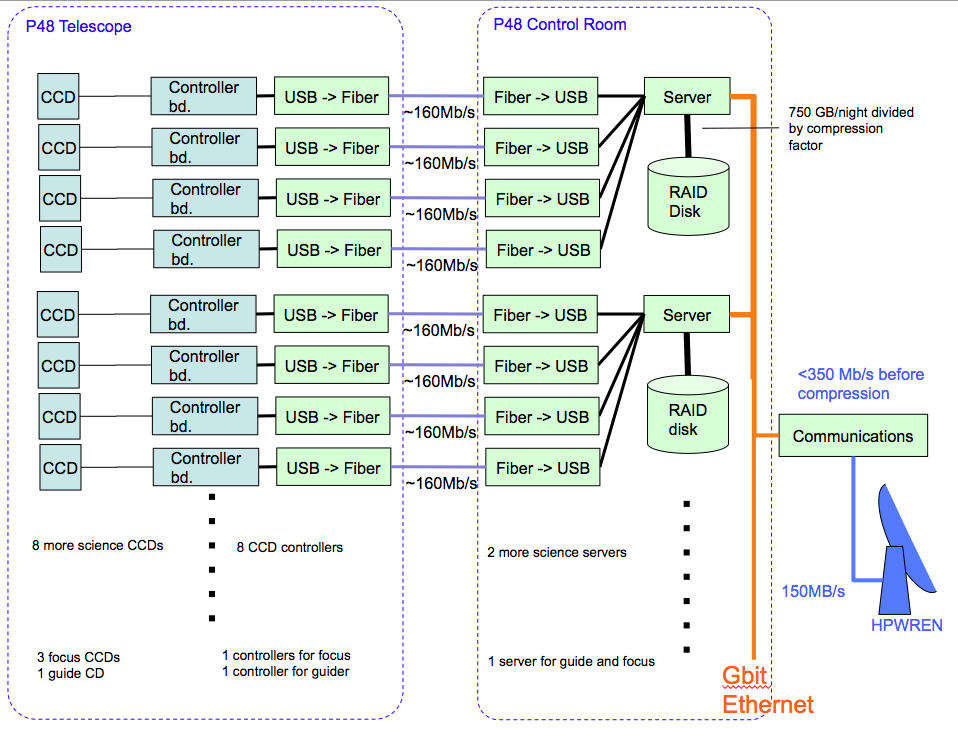


Figure 1: Data paths. Each 4 channel CCD is serviced by a single board controller (SBC). Each communicated by a USB2 datalink to the host via fiber optic USB2 extender. The number of USB2 links will be determined by tests of supported data rate.

The mapping of a single board to one CCD is optimal from the point of view of grounding and to minimize crosstalk (see the grounding discussion on page 34). The loss of one controller only affects one CCD, and the system is easily extended, but is presently set to 20 controllers for ZTF. All boards are inter-changeable without any reconfiguration, and all customization is through programmable features or jumpers/wiring on the backplane, thus installation of spares is simple.

# Performance Table

Programmable Biases

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Minimum | Maximum | Note |
| Number | 16 |  |  |
| Voltage Range | 0 V | 35 V | Requirement driven by Output Drains |
| Resolution | 12 bits |  |  |
| Current | 20 mA |  | OS and DOS ganged with safety factor 2 |
| Noise |  | 184 uV | How is MOSFET gain affected by Vds noise? |
| Drift | TBD |  | By temperature? Will investigate typical temp change in a night |
| PSRR | 85 dB |  | Assuming Vicor DC power supply with 1.0% Vout ripple |

Table 1: Programmable Biases Performance

Programmable High Voltage Bias

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Minimum | Maximum | Note |
| Number | 1 |  |  |
| Voltage Range | 0 V | -60 V | Requirement driven by guider/focus CCDs |
| Resolution | 12 bits |  |  |
| Current | 20 mA |  |  |
| Noise |  | 184 uV |  |
| Drift | TBD |  | By temperature? Will investigate typical temp change in a night |
| PSRR | 85 dB |  | Assuming Vicor DC power supply with 1.0% Vout ripple |

Table : Programmable High Voltage Bias

Serial Clocks

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Minimum | Maximum | Note |
| Number | 10 |  |  |
| Voltage Range | 0 V | 14 V |  |
| Resolution | 10 bits |  | Goal of 12 bit resolution |
| Current | 100 mA |  | Required for 60 ns risetime on Register clock phase 1 ganging |
| DAC write time |  | 2 u sec | Initialized at turn on. Fast write time not as critical. |
| Settling Time |  | 70 ns | From mux switch to 0.1% of voltage |
| Noise |  | 50 uV | Bandwidth of clock is 6.4 MHz |
| Drift | TDB |  | Temperature? |
| PSRR | 85 dB |  |  |

Table 3: Serial Clock Performance

Parallel Clocks

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Minimum | Maximum | Note |
| Number | 10 |  |  |
| Voltage Range | 0 V | 14 V |  |
| Resolution | 10 bits |  | Goal of 12 bit resolution |
| Current | 15 mA |  | Risetime is 100 us as per tri-level clocking scheme |
| DAC write time |  | 2 u sec | Acceptable if multiple channels can be written in parallel |
| Settling Time |  | 105 usec | From DAC load to 0.1% of voltage |
| Noise |  | 50 uV | Bandwidth of clock is 3.5 kHz |
| Drift | TBD |  | Temperature? |
| PSRR | 85 dB |  |  |

Table 4: Parallel Clock Performance

Video

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Minimum | Maximum | Note |
| Number of Channels | 4 |  |  |
| Gain | 1 | 1 | Fixed gain on controller |
| Noise |  | 375 µV | At ADC input |
| Buffer Offset | 4.096 V |  | Allows for inverting single ended signal |
| Buffer Anti-aliasing Filter | 20 MHz |  | Bandwidth is 2x sampling frequency |
| ADC Throughput | 10 MSPS |  |  |
| Correlated Double Sampling | - | - | Must be done digitally |

Table 5: Video Performance

Data Link Rates

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Minimum | Maximum | Note |
| Number of Channels | 1 |  | Data link is USB 2.0 |
| Data Rate | 130 Mbps | 480 Mbps | Minimum data rate for 1MHz pixel rate, 32 bit data |

Table 6: Data Link Performance

Power Supply Requirements

|  |  |  |  |
| --- | --- | --- | --- |
| Voltage | Current | Noise (rms) | Note |
| +36 | TBD | 0.36 V | Analog voltage |
| +15 | TBD | 0.15 V | Analog voltage |
| +5 | TBD | 0.10 V | Analog voltage |
| -5 | TBD | 0.10 V | Analog voltage |
| +15 | TBD | 0.15 V | Clock voltage |
| +5 | TBD | 0.10 V | Clock voltage |
| -5 | TBD | 0.10 V | Clock voltage |
| 3.3 | TBD | 0.10 V | Digital voltage |

Table 7: Power Supply Requirements

# Timing Generator

The state machine for the sequencer is independent of the application. The FPGA “programming” will be independent of the sensor readout algorithm once the correct set of tools has been provided.

The controller has no built in “read modes” which are specific to any CCD or readout algorithm. Instead the sequencer generates readout functions in response to timing definitions downloaded to FPGA’s RAM these timing definitions will be simple tables as illustrated below.

[Details of this description may be changed to simplify the FPGA design but the general concept is likely to survive.]

A series of tables are downloaded by the host into FPGA into memory. Entries in these lookup tables or the current values in “variables” can be modified on the fly by the host to alter the behavior of the controller. The host can also read back any of these parameters both for diagnostics and to monitor the current status of the controller.

To initiate a readout the host processor writes an initial instruction pointer to address the first entry of the highest level “table”.

Each line of a table has up to 4 fields:

1. The command field defines what to do. The number of bits needed depends on the number of command options we define. 4 bits will probably suffice. The meaning of the remaining fields depends on the command decoded.
2. Address of DAC or register to be accessed, if applicable.
3. Data value or pointer to another list.
4. Repeat counter or time delay. The units for the delay time may depend on the command.

Let’s consider a simplified example where 100 exposures each 2s long are executed and each time only a 7\*8 pixel ROI is read out at coordinate 100,200 on a single channel CCD which is 1000 pixels square. To simplify this

**Start:**

|  |  |  |
| --- | --- | --- |
| Wait for external trigger | NA | NA |
| Repeat | Frame | 100 |

**Frame:**

|  |  |  |  |
| --- | --- | --- | --- |
| Write | Shutter | 1 | 0 |
| Repeat | Wait for millisec | 2000 | |
| Write | Shutter | 0 | 0 |
| Repeat | Wait for millsec | 50 | |
| Repeat | ROI | 1 | |

**Wait for millisec**

|  |  |
| --- | --- |
| Wait | 100,000 |

**ROI:**

|  |  |  |
| --- | --- | --- |
| Repeat | Skip Line | 199 |
| Repeat | Serial Shift | 1000 |
| Repeat | ROI line | 8 |
| Repeat | Skip Line | 800\* |

\* Erasing slightly more than the full CCD area.

**Skip Line:**

|  |  |  |
| --- | --- | --- |
| Repeat | Parallel Shift | 1 |
| Repeat | Skip Pixel | 100 |

**ROI line:**

|  |  |  |
| --- | --- | --- |
| Repeat | Parallel Shift | 1 |
| Repeat | Skip Pixel | 99 |
| Repeat | Read Pixel | 7 |
| Repeat | Skip Pixel | 894 |

**Parallel Shift:**

|  |  |  |  |
| --- | --- | --- | --- |
| Write DAC | DAC # | <value> | <delay> |
| Write DAC | DAC # | <value> | <delay> |
| Write DAC | DAC # | <value> | <delay> |
| etc |  |  |  |
|  |  |  |  |

Note: the units for the delay after a DAC write do not have to be the same as that for the delay after writing a “state”. It would be a good idea to have a prescaler in the case of the “DAC\_delay” since these delays are used for parallel clocks which are much slower than the “state\_delay” used for pixel timing.

**Skip Pixel:**

|  |  |  |  |
| --- | --- | --- | --- |
| Write | <register> | <bit pattern> | <delay> |
| Write | <register> | <bit pattern> | <delay> |
| Write | <register> | <bit pattern> | <delay> |
| etc |  |  |  |

Partition the signals into output registers which have some logical association (eg all serial clocks) and which will be updated simultaneously, while having separate “addresses” for bits that control logically independent functions which do not have to be updated at exactly the same time as bits in other output registers. In this way one can write to one group of bits without having to worry about defining/preserving the state of the others.

The outputs controlled by the “bit pattern” will include analog switch control lines for selecting clocks for fast clocks like serials, summing well and reset gate, as well as logic level (LVDS) outputs for black level clamp, scope trigger, shutter control etc, and internal logic signals such as ADC start convert, and data transfer strobes, artificial data counter clock, etc. By using the “sequencer” to program these internal control signals as well as those that go to the CCD, the readout timing is as flexible as possible.

**Read Pixel:**

|  |  |  |  |
| --- | --- | --- | --- |
| Write state | <register> | <bit pattern> | <delay> |
| Write state | <register> | <bit pattern> | <delay> |
| Write state | <register> | <bit pattern> | <delay> |
| etc |  |  |  |

The “delay” here sets the timing resolution for the pixels. With 1µs/pixel we would like ~10ns resolution. Ideally a delay of zero would produce 10ns time between updating states, but 20 ns would be tolerable for the minimum state time.

How fast can we update states, without invoking a FIFO. It is best to avoid a FIFO since it will create the need for sensing whether FIFO is full and when it goes empty and one can proceed to the next operation (assuming it needs to be synchronized).

Care will be required in the design to support the nesting of loops as called for here. The common solution to this problem is to reuse registers for loop counters storing the present register value to a memory stack whenever a new loop counter is loaded. Nesting depth of at least 6 is required, so 8 would be safe.

The most critical overhead is that which occurs between each pixel. Overheads for looping need to be kept down to only a few time resolution elements, or (ideally) be completely hidden by pipelining. It would be good to do repeat count decrement and test (determining next instruction) in the same cycle as executing a write of the new state. One would then only “see” the loop overhead where an outer loop is processed as well as the inner loop.

There are other design options where different repeat counters can be used. Instead of the command being “repeat” it becomes a set of commands “Repeat 1”, “repeat 2”, etc, each of which uses a different loop counter. This avoids the time over head of stack processing and may be preferable.

When discussing these finer points of the design we need to consider how to generate waveforms in which the parallel and serial clocks are being up dated ***concurrently.***  This will be required to support new clocking modes, which minimize charge trapping in the columns by spreading much of the parallel transfer out across the total line time. In an FPGA based sequencer it is reasonable to create separate state machines for the pixel and line timing with signals between them to allow one to wait upon the other at, for example, line start. To simplify the example above this capability has not been illustrated.

Other sequencer commands that might be useful are:

* Set/clear/increment/decrement counter (which can be read out by the host)
* Wait for, set, clear flag (which host can also test/set).
* Ditto for signals to synchronize pixel and line sequencers.

These options are open for further discussion, and space on the front panel should be made for diagnostic signals of these types.

# Serial Clock Drivers

Serial clock drivers will generate all clocks involved in pixel timing: serial register clocks, Summing Well, and Reset Gate.

To support 1 megapixel per second readout with 3 phase serial clocks we need rise and fall times to be <~ 60 ns (see Figure 2 for pixel timing waveform) for a maximum load 600 pF, which corresponds to two phase 1 serial clocks ganged on an e2v CCD 231-C6.

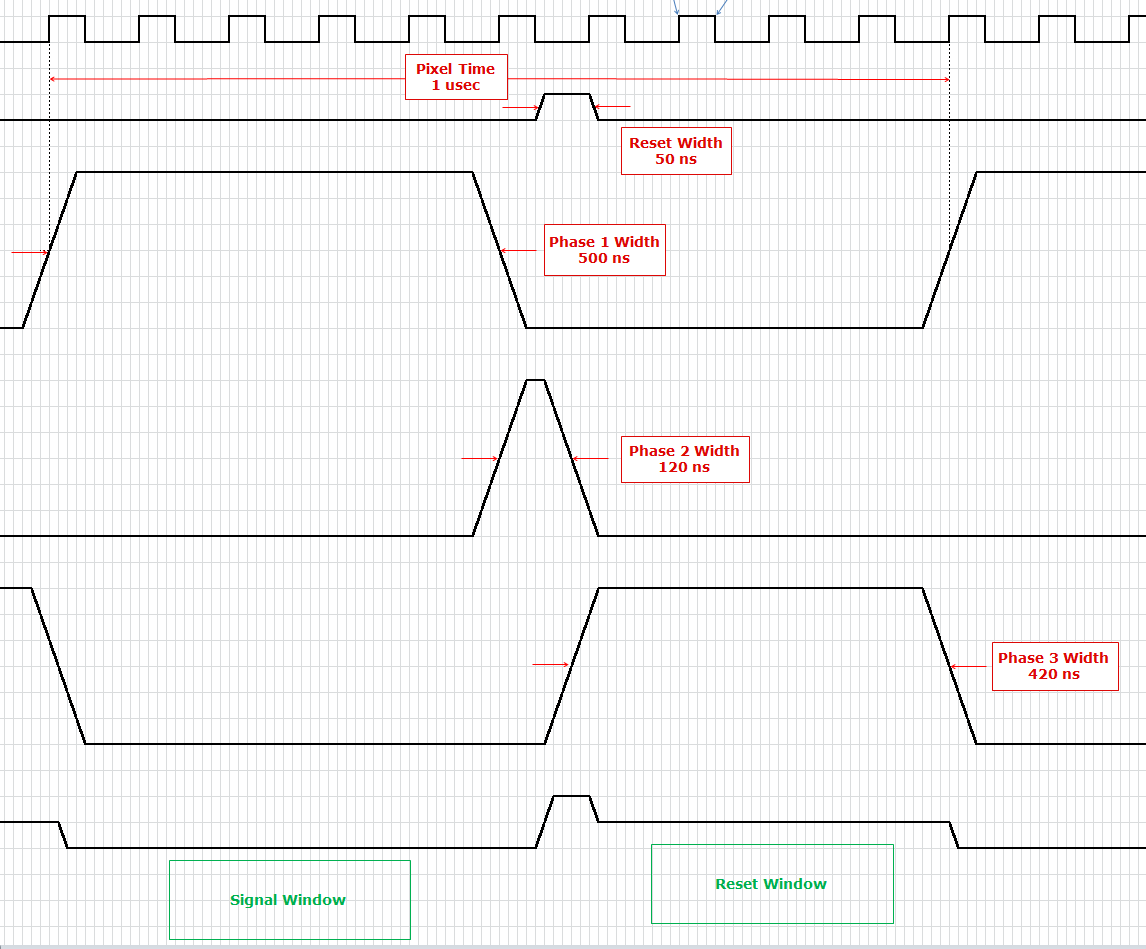


Figure 2: Timing Waveform Single Pixel

To accommodate this clock rate the conventional architecture will be adopted wherein analog switches, controlled by the sequencer described above, select between two fixed programmable voltages (>10 bit DACs, prefer 12 bit) whose values can also be written by the sequencer if levels need to change at some point during readout.

The analog switch, which selects between DACs is followed by a buffer which provides the drive current. This buffer can have some gain so that the clock swing can exceed the DAC range if necessary. The DACs can drive the switch directly since load capacitance into the switch and buffer input will be low.

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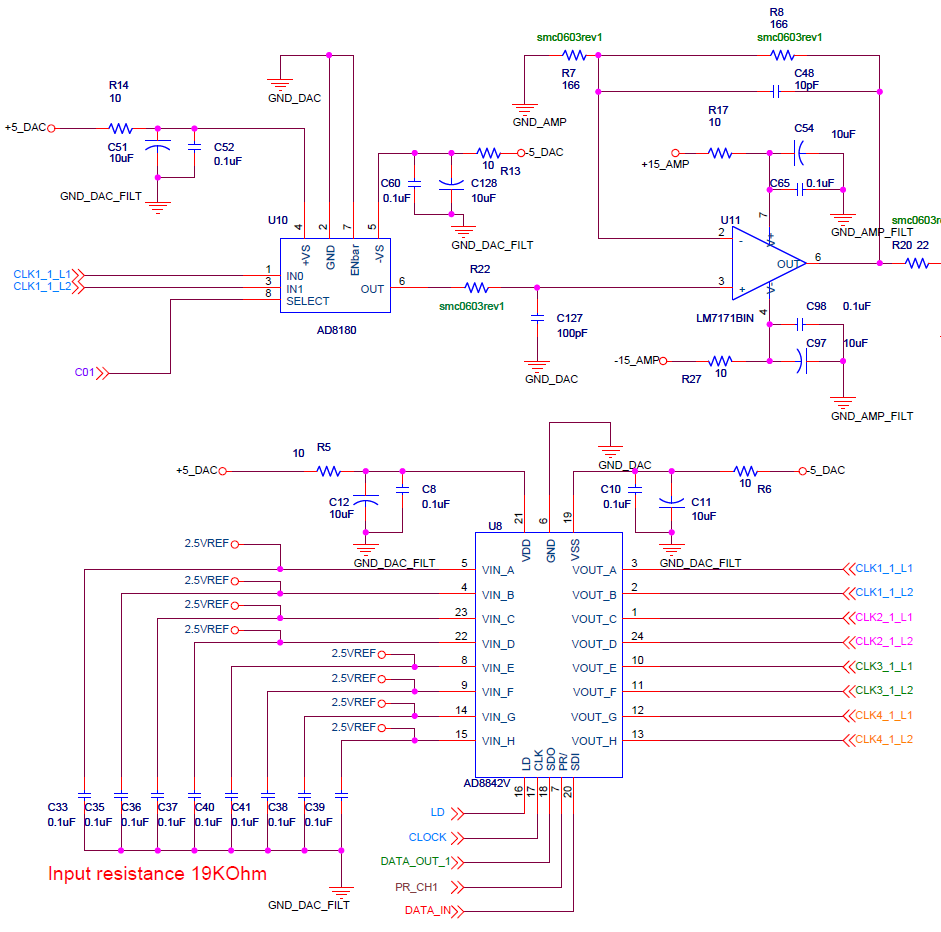


Figure 3: Serial Clock Driver

The present clock driver has sufficient drive current for the application. Recent measurements made on the prototype card show a rise time of 73 ns for a load capacitance of 680 pF and a 10 V signal swing. For a 600 pF load, this rise time should be approximately 64 nsec which is slightly under specification. An isolation resistor on the output for driving a capacitive load may limit the rise time of the pulse and require the use of a different op-amp.

The power required for the present driver is ~174 mW per clock. For a full complement of clocks (20), the power

required is 3.5 W which is reasonable for the serial clocks. It is anticipated that designing the serial clocks for unipolar operation will further reduce the power consumption.

# Parallel Clock Drivers

The parallel clocks can be driven by the same op amp as the serials. While the capacitive loads are higher, up to 110 nF for two CCD 231-C6 parallel phases ganged, the rise time requirement is looser, <100 µs.

We propose a more modern approach to Parallel Clock Drive wherein the timing generator writes new values to the parallel clock DAC to change clock states. This reduces the number of DACs per clock from two to one and eliminates the analog switch and logic that selects between them, with consequent power and space savings.

Clocking will be concurrent with line readout instead of being inserted between line reads to allow slower rise times which reduces clock drive current requirements so that large capacitances can be more easily driven. This architecture also supports a newly discovered “slow tri-level clocking” method which mitigates charge traps and thus improves charge transfer efficiency.

The time to update multiple DACs will create timing skew which could become objectionable. The ideal solution is to find serial DACs, which allow a value to be shifted in but not broadside loaded until a strobe is received. This would allow new values for multiple DACs to be loaded then for all new values to take effect simultaneously. If this is not available then a sufficiently fast update rate (say <200ns per DAC) would keep skews under control. At most 10 DACs would be updated at once; with rise times exceeding 40 µs, skew would be less than 5% of rise time.

**The circuit for the parallel clocks would be similar to what has been proposed for the prototype clock driver without the 2:1 multiplexer. The careful design of the circuit must not allow glitches on the clock line when the DAC value is changing**.

Parallel and serial clocks would have separate timing generators which would each be able to wait for a synchronization signal form the other to enforce sequential operation when needed, typically once per line.

**Clock and bias drivers must be frequency compensated to be able to drive large capacitive loads without oscillation or overshoot. This series impedance (some inductance as well as resistance for a critically damped LCR output impedance) in this circuit can provide superior isolation from high frequency noise coupling from power supplies (particularly useful when using switching power supplies).**

# Substrate Driver

Substrate will be actively driven in the manner advocated by e2v. (The low rail of the parallel clocks is nominally zero volts.) This allows all clocks to be shifted relative to substrate by adjusting one voltage (the substrate) instead of many (the clocks) to move between clock inversion (for low dark current and no image persistence) and maximum electric field penetration (all clocks positive relative to substrate) for low lateral charge diffusion.

Since a substantial fraction of the clock capacitance is to substrate, the substrate driver will share the same power supplies and ground as the other parallel clocks, rather than the bias driver ground. For this reason, the substrate driver will use a serial clock circuit which will not be switched.

Due to all of the clocks being capacitively coupled to the substrate, the substrate will require a higher current sink capability. The current through the substrate can be kept low by synchronizing the rise and fall times of clocks as seen in the timing diagram in Figure 2. For this reason, the current capability of the substrate bias must be TBD times higher than any serial clock

# Bias Drivers

Bias drivers differ from clock drivers primarily by having different output ranges and may have heavier output filtering and thus slower response to DAC changes. Bias drivers must be frequency compensated for capacitive loads not so much because the CCD load is highly capacitive but because a large output filter capacitor will be used. An example of the frequency compensated topology is shown in Figure 5. The series resistor for this RC filter is inside the feedback loop so that the bias driver has low output impedance at low frequencies. At high frequencies this RC provides passive filtering and thus immunity to power supply switching noise (etc).

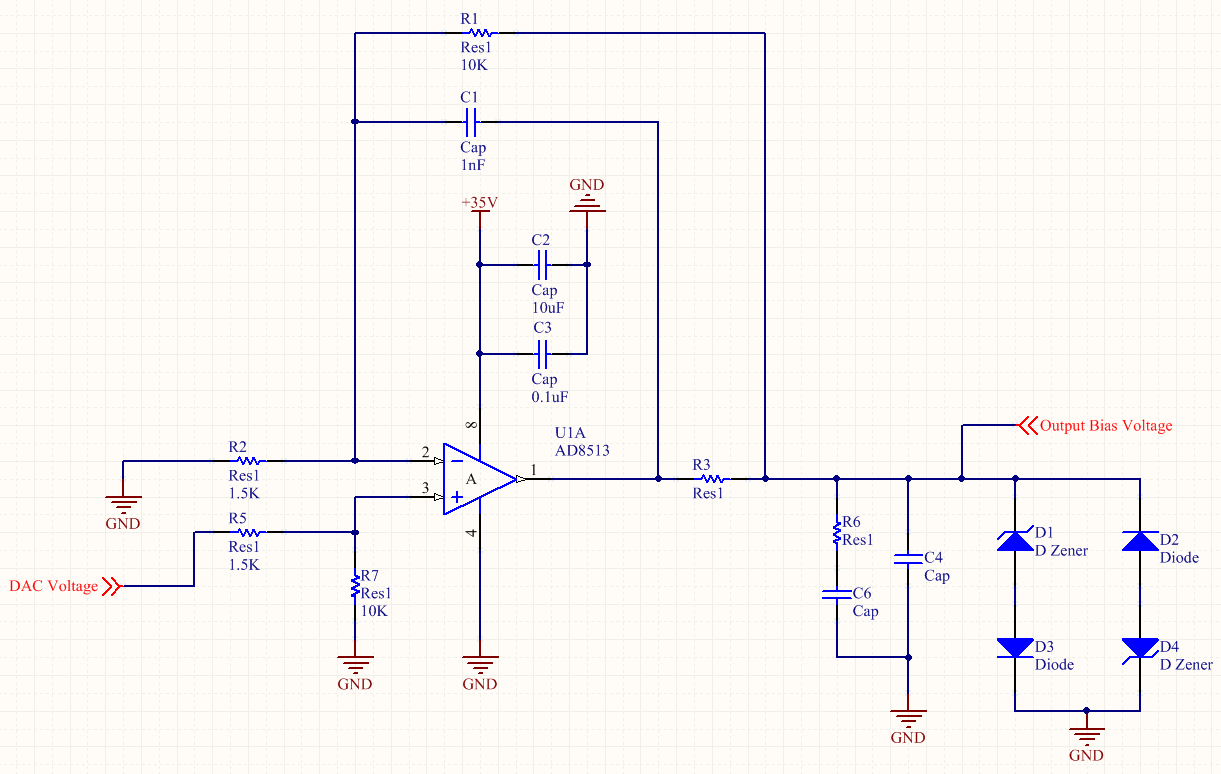


Figure 4: Bias Voltage Example Circuit

A minimum of 16 output biases are needed with a voltage range from 0 V to 35 V, and an extra negative high voltage output is needed for the backside contact of the delta doped guider/focus CCDs.

The need for voltages up to 35 V is mainly driven by the needs of the output drain of the CCD’s amplifier. Additional voltage is needed since the substrate will be driven by a voltage higher than 0 V. The resolution for the bias drivers needs to be 12 bits. This resolution will allow adjustment on an 8.5 mV scale. A lower resolution will not have the granularity of control which is needed to optimize the CCD. Table 7 shows a list of specific biases which will be needed, but the voltages are the nominal voltages for a substrate voltage of 0V. The voltages may need to be adjusted for operational mode and/or optimization. Note: This table groups by function but is not necessarily the actual pinout which will be used. Any substrate voltage will adjust the nominal voltage up by the value of the substrate voltage.

|  |  |  |
| --- | --- | --- |
| Reference | Function | Nominal Voltage |
| OG-E, OG-F, OG-G, OG-H | Output gate | 2 V |
| DOD-E, DOD-F, DOD-G, DOD-H | Dummy Output Drain | 27.5 V |
| OD-E, OD-F, OD-G, OD-H | Output Drain | 27.5 V |
| RD-E, RD-F, RD-G, RD-H | Reset Drain | 17 V |
| DD-A, DD-D | Dump Drain | 26 V |

Table 8: Bias Functions and Nominal Voltages

The noise on the bias drivers is most crucial for the Output Drain and Dummy Output Drain voltages. The noise on the bias voltage for the output amplifier will have a direct effect on the noise of the output signal. Looking at the error budget and knowing that the noise at the ADC needs to be around 3 LSB (375 µV), the limit on the noise contribution from the bias drivers can be found. The CCD source follower and the preamplifier contribute 148 µV of noise to the signal, and the post processor buffer to the ADC contributes 43 µV of noise to the signal. This leaves a noise budget of 184 µV from the output drain bias voltage. A worst case assumption is made that the voltage noise on the drain voltage couples directly to the video signal. With this assumption, the maximum allowable noise on the bias driver is 184 µV. The bias noise present on the output drain and the dummy output drain are correlated and so the √2 penalty does not apply for the differential signal. Please refer to the the preamplifier noise section on page 16 and the post processor noise section on page 21 for a detailed analysis of the noise contributions from those sections of the circuit. An analysis of this type is expected for the final bias circuit.

# The negative high voltage is needed for the backside bias for the delta doped guider and focus CCDs. The guider and focus CCDs are thicker devices with a dopant implantation at the backside interface. This dopant implantation forces charges near the surface into the CCD and due to its thickness, an additional voltage is needed to propel the charges into the charge wells provided by the image clock voltages. An appropriate op-amp must be selected to handle the high voltage and a voltage doubler is used to bias the high rail of the driving op-amp. A DC-DC converter such as Texas Instrument’s DCP02 can be used to generate the high voltage rail for a driver op-amp.Video Processor

## Differential Video

CCD signal paths are usually single sided since the second transistor in a matched pair will exhibit similar noise and thus total noise is increased by √2. However in ZTF sky noise is dominant and differential transmission has many other advantages which address the problems associated with the higher noise bandwidth required by the high pixel rate:

* Crosstalk immunity
* Immunity to RF interference.
* Better power supply rejection ratio throughout.
* Bias noise and drift becomes common mode and are rejected.
* Rejection of clock and reset feedthrough: faster settling after these transients. This will suppress fixed patterns, particularly line start transient.
* AC coupler drift becomes common mode so that black level clamping can occur once per line and be hidden within the parallel shift.
* Simplicity: fast ADCs require differential inputs anyway.

These advantages will not only provide lower noise and fixed patterns, and less crosstalk, but the performance of clock and bias drivers becomes less critical.

By providing independent control signals for the signal and reference AC coupler black level clamps, we can short out the noise in the reference side, giving up rejection of bias and clock feedthrough but preserving immunity to noise and crosstalk occurring downstream of the preamp. This might be invoked for a slower scan low noise readout option. This is not required in ZTF at present, but could be useful for narrow band or UV imaging in WaSP where sky noise may be sub dominant.

The science CCDs, e2v 231-C6, offer dummy outputs, which provide the reference side for the differential signal transmission. The guide and focus CCDs do not have this feature but we can use the output at the opposite end of the same serial register provided that we can accept reading form only one output per serial register. This is probably so, but needs to be considered more carefully. Choosing to read from the other end will of course swap the signal and reference inputs and result in a negative going signal voltage being presented to the unipolar ADC. This could be dealt with by adjusting the output offset DAC to present (nearly) the most positive voltage to the ADC when there is no signal present and then decreasing voltages as the signal increases. (Our NIR controllers happen to work this way). The polarity can then be corrected in the Digital CDS processing.

## Preamp on VIB

The preamplifier is located as close as possible to the CCD flex circuit, i.e. within the vacuum, on the Vacuum Interface board. It operates slightly below room temperature where leakage currents will be lower and the VIB will radiate less power into the back of the CCD mount. Ideally this components would be rated for e “industrial temperature range” and operate at around -20C providing ample margin to the -55C lower limit. A schematic of the preamplifier circuit can be found in Figure 6.

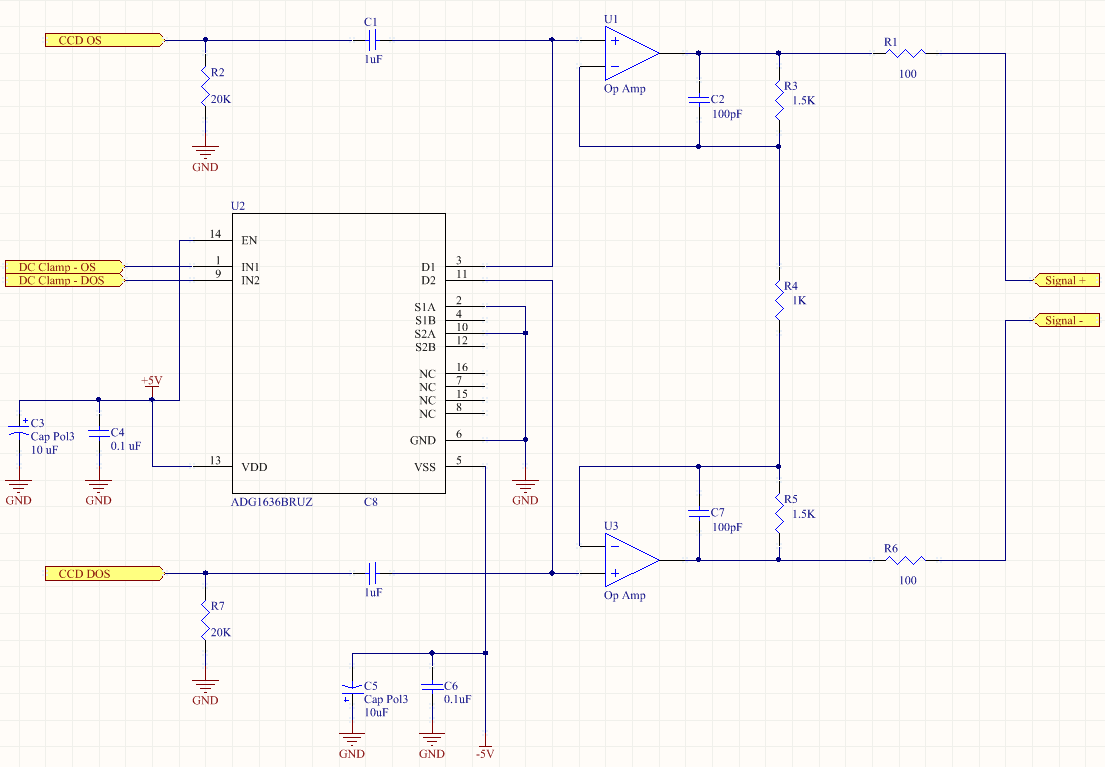


Figure 5: Preamp Schematic

Matched AC couplers are provided for the signal and reference paths with separately controlled analog switches in place of the resistor normally found in an AC coupler. These will be closed during parallel shift to re-establish the DC input level. The symmetry of the circuit and careful layout of the PCB for temperature matching should match the drifts at the preamp inputs so they cancel.

The preamp is a classic differential pair, which has unity gain form common mode signals and greater than unity gain (about 4 in this case) for the differential component.

For Digital CDS, gain can be fixed for any given CCD since it depends only on well capacity and CCD output node sensitivity. Unlike conventional dual slope CDS circuits neither preamp nor integrator gain needs to be adjusted when integrating to reduce noise bandwidth. Since the gain setting is in the preamp and this is located in vacuum close to the CCD, the gain setting is embedded in the dewar with the CCD and the portion of the video chain in the controller has unity gain, and needs no gain adjustment capability.The video signal gain is chosen with regard to the full well of the CCD and the differential input voltage range for the video board analog to digital converter. The full well for the CCD will be 275,000 e- which will be mapped to 60,000 ADU. This gives a conversion gain of 4.6 e-/ADU. The analog to digital converter currently selected (AD7626) is a 16 bit ADC with a differential input voltage range of +/- 4.096 V. This gives a voltage conversion of 125 µV/ADU. Using the CCD sensitivity of 7 µV/e-, the calculated desired signal gain is

This gain is completely implemented in the pre-amplifier stage for this design and subsequent stages must have a gain of one.

To arrive at a gain of 4, resistors R3, R4, and R5 are chosen according to the equation:

This equation is true for the circuit when R3 is equal to R5. For the preamplifier, R4 is chosen as 1 kΩ and R3 and R5 as chosen as 1.5 kΩ. A 100 pF capacitor is placed in the feedback loop of each op-amp to filter out unwanted higher frequencies and improve stability.

The noise on the signal can be found by adding in quadrature the various random and uncorrelated sources. These contributions come from the CCD on-chip source followers, load resistors, the instrumentation op-amps, and the resistor thermal noise.

The on-chip amplifier noise can be found from the chart provided by e2v in Figure 7, where the frequency versus output noise in electrons is shown. Running the CCD at 1 MHz results in an output noise of 5 e-. **This noise appears on both the true output and the dummy output. Since these signals are used differentially, and their noise components are uncorrelated, they add in quadrature, which results in an extra factor of √2 for a noise contribution of 7 e- from the on-chip source follower.**

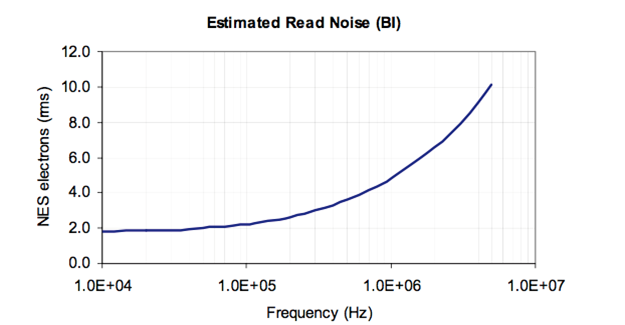


Figure 6: CCD On-Chip Amplifier Noise

To convert this total noise to an input referred voltage noise density one integrate the noise power spectrum times the frequency response of the correlated double sampler. To get a rough idea of the op amp noise specs we will assume a rectangular (flat) band pass cutting off at flow = pixel rate/2 and fhigh= 2\* pixel rate, so noise bandwidth, B = 1.5MHz.

It appears from the noise curve below that the e2v CCD noise corner frequency is somewhat below 1MHz and the Op Amp selected should have a noise corner well below 50KHz, so we will assume a white noise spectrum in both cases. Thus noise density for the CCD is

The sum of the following noise sources should be kept well below this level. The total noise budget is allocated in Table 8. **Note is a differential circuit all noises are incurred twice unless noted. The single sided noises are calculated below.**

In the CCD reset switch resistance, referred to a KTC noise need not be considered since it is removed along with any low frequency drift of biases by the CDS process.

Similarly the KTC noise on the black level clamp is removed by the CDS processing.

### CCD source follower load resistor thermal noise

The thermal noise density of a resistor is given by the equation with units of V/√Hz . For a 20 kΩ source follower load resistance at 295K, this gives a noise density of 18 nV/√Hz. However, this has to be divided by the potential divider formed by the CCD output impedance (7Kohm to 5Kohm) and the load resistance, to the Thevenin equivalent noise voltage of

### Op amp feedback resistor thermal noise density

The thermal noise density for the 1.5 kΩ feedback resistor is 4.9 nV/√Hz. This is the noise at the output and must be divided by the gain of 4 for an input referred noise of 1.2 nV/√Hz.

### Op amp bridging resistor thermal noise

The thermal noise density for the 1 kΩ resistor is 4 nV/√Hz. Note that this is already input referred and is only incurred once.

### Op Amp input voltage noise

The currently selected op-amp (OPA354) has an input voltage noise of 6.5 nV/√Hz.

### Op amp input current noise

The currently selected op-amp has an input current noise of 0.05 pA/√Hz. Given the parallel combination of the 20 kΩ load resistor and the 7 kΩ source impedance, the voltage noise is calculated to be 0.26 nV/√Hz.

### Black level clamp leakage current noise.

The currently selected switch (ADG1636) has a maximum leakage current of 2 nA over the desired temperature range. The poisson current noise is given by

With a 20 kΩ CCD source follower load (the largest contemplated) and a 7 kΩ output impedance, the leakage current generates a voltage noise at the input of 0.125 pV/√Hz. This contribution to the input referred noise is negligible.

|  |  |  |
| --- | --- | --- |
|  | Input Referred Noise | Voltage Noise |
| CCD Source Follower | 40 nV/√Hz | 40 nV/√Hz |
| Source Follower Load Resistor | 4.7 nV/√Hz | 4.7 nV/√Hz |
| Op-amp Feedback Resistor | 1.2 nV/√Hz | 1.2 nV/√Hz |
| Op-Amp Bridge Resistor | 4 nV/√Hz | 4 nV/√Hz |
| Op-Amp Input Voltage Noise | 6.5 nV/√Hz | 6.5 nV/√Hz |
| Op-Amp Input Current Noise | 50 fA/√Hz | 0.26 nV/√Hz |
| Clamp Leakage Current Noise | 25 fA/√Hz | 0.125 pV/√Hz |

Table 9: Preamplifier Noise Sources

Total noise can be calculated by adding all of the contribution in quadrature, and ignoring the insignificant contributions. All of contributions are found in Table 8. Note that all contributions except for the bridge resistor have an extra √2 penalty due to the differential nature of the circuit.

# Using a bandwidth of 1.5 MHz, we have a total noise of for the preamplifier.Digital CDS

The Digital CDS approach to be used is gaining in popularity with the advent of fast low power 16 bit ADCs. It offers the following advantages:

* Much simpler analog circuitry. In exchange, some digital processing is required but this is well within the capability of typical FPGA’s already incorporated.
* No gain changes or analog bandwidth adjustment when changing pixel rate. Very useful for WaSP where sky background (thus read nosie requirements) will change drastically among filters.
* Numerical resolution is increased beyond that of the AD converter so that the full CCD dynamic range can be supported without resorting to 18 or 19 bit ADCs. This important for the very high well capacity of the CCDs used in WaSP and ZTF.
* Provides very high-speed readout, without any adjustments, when noise is not an issue. Useful for scene preview, focusing etc.
* Supports “digital oscilloscope mode” at normal pixel rates providing an excellent remote diagnostic capability.

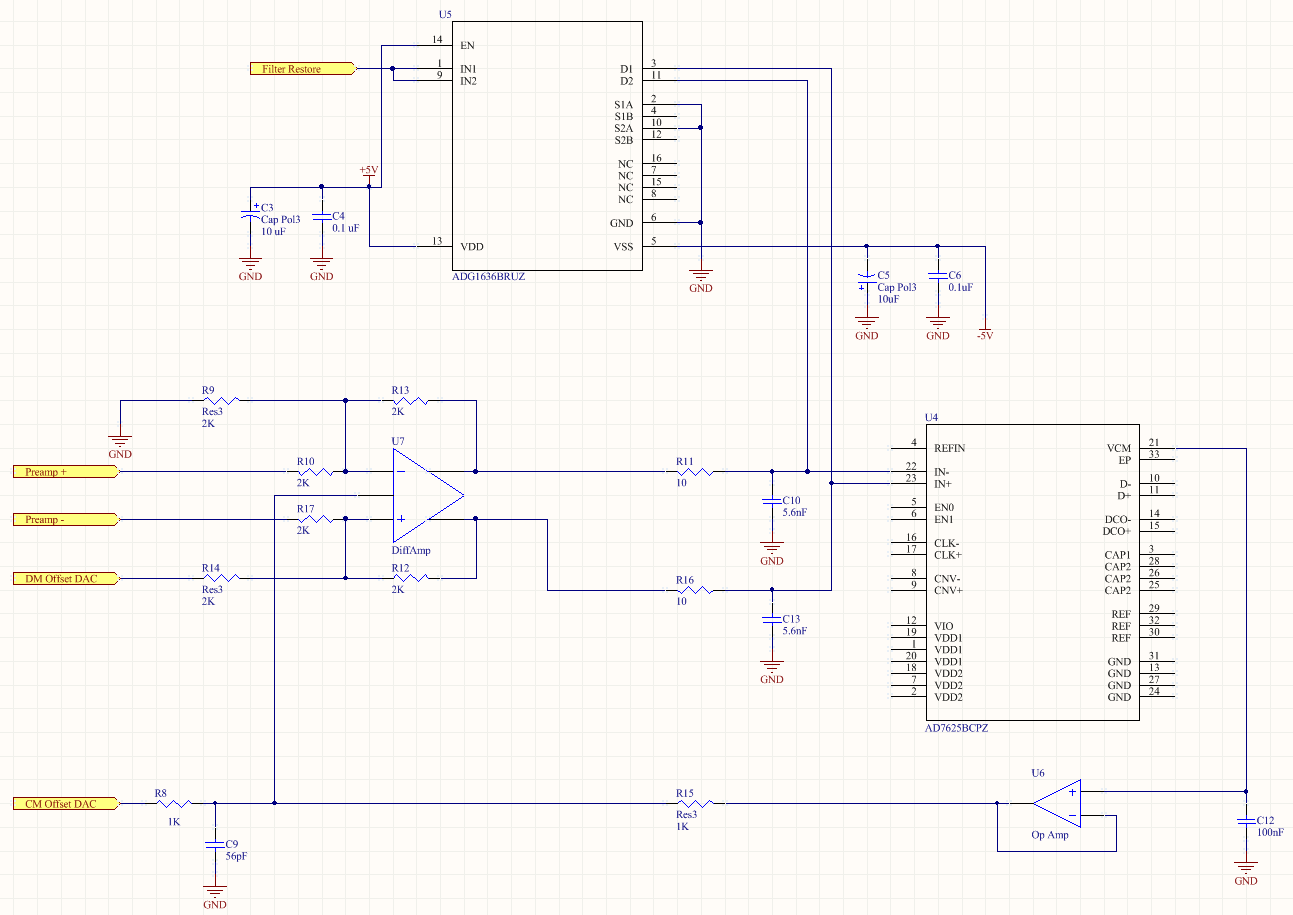


Figure 7: Video Processor

The Digital CDS circuit shown in Figure 8 is a simple unity gain differential ADC driver and differential 10 MSPS ADC. An output from the ADC nulls the common mode component.

A DAC provides a programmable differential offset which enables the full ADC signal range to be used in the presence of an intrinsically unipolar signal differential signal. This differential offset needs to be inserted into one side of the differential amplifier and must have a range of 4.096 V to -4.096 V. This voltage range will allow for an inversion of the signal if a single sided mode is selected at the preamp. An additional DAC is supplied to the common mode adjustment pin to enable optimization of the common mode signal. The elimination of this adjustment can be considered due to the ability of the ADC to feedback a proper common mode voltage.

A subtle but key feature is the anti-aliasing filter whose corner frequency is set near the Nyquist frequency. It may be set slightly above Nyquist to provide faster settling time if the extra noise bandwidth is found to be minimal. With a 10 MSPS ADC and 1 MHz pixel rate, Nyquist is only 5 times the pixel frequency so there will be substantial settling occurring on the scale of a pixel. To minimize pixel to pixel crosstalk due to settling, a *fast* analog switch resets the differential component of the signal after the antialiasing filter (shorts both) sides together. This can occur during the CCD reset and thus be hidden.

The FPGA will average the samples of the post reset level and subtract these from the average of the level after change dump. The triggering of the samples will be programmed along with other aspects of the pixel timing. After averaging and subtraction, the data will be transmitted as a 32 bit signed integer. This is more numerical resolution than will ever be needed, but it assures that the data is stored on the host in a format that is amenable to compression without having to be “unpacked” form a denser custom format. **We have enough throughput in the USB2 link to support this “padding” to 32 bits.**  Since we have resolution to spare, the FPGA can use a 32 bit accumulator and never needs to normalize the data after subtraction.

For diagnostics, the FPGA must also support pass through of raw data and the generation of artificial data. Artificial pixels will be a fixed code written by the host, usually a different value for each CCD channel and a counter. With a 32 bit word, we could reserve 7 bits for 256 channel identifiers, then have 24 bits for the counter that is reset at frame start and produces a unique value in every pixel.

A systematic review of the noise sources can provide a basis for the calculation of the total noise from the ADC buffer. The noise sources are from the amplifier itself in terms of input voltage noise, input current noise, and common mode voltage noise. The surrounding components also contribute to the noise, i.e. the feedback resistors and gain resistors. A model of the noise sources is shown in .

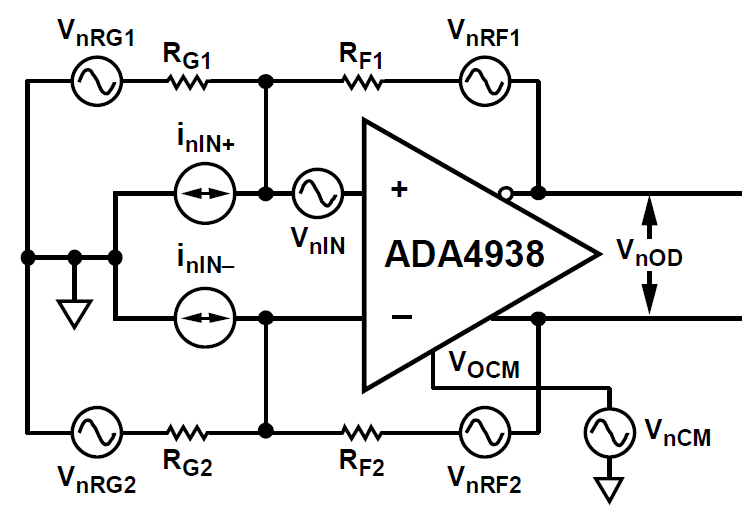


Figure 8: Noise Source Model

The input voltage noise (VnIN), input current noise (InIN+ and InIN-), and common mode voltage noise (VnCM) are all properties intrinsic to the differential amplifier. The value of these sources of noise can be found in the ADA4938 data sheet and are entered in .

|  |  |  |  |
| --- | --- | --- | --- |
|  | Input Voltage Density (nV/√Hz) | Output Multiplication Factor | Output Voltage Density (nV/√Hz) |
| Differential Input | 2.6 | GN | 5.2 |
| Inverting Input | 4.8 | GN | 9.6 |
| Noninverting Input | 4.8 | GN | 9.6 |
| Vocm Input | 7.5 | GN(β1 – β2) | 0 |
| Gain Resistor R10 | 5.74 | GN(1 – β1) | 5.74 |
| Gain Resistor R17 | 5.74 | GN(1 – β2) | 5.74 |
| Feedback Resistor R13 | 5.74 | 1 | 5.74 |
| Feedback Resistor R12 | 5.74 | 1 | 5.74 |

Table 10: Differential Amplifier Noise Sources

The total output voltage density from the ADC buffer is the square root of the sum of squares of all of the contributions.

For completeness, the single pole RC filter after the buffer amplifier must also be considered in the noise calculation. Specifically, the two resistors (R11 and R16) contribute thermal noise to the input of the ADC.

This level of contribution is small compared to the buffer amplifier and its components and can be safely ignored.

Using a bandwidth of 1.5 MHz, we have a total noise of for the ADC buffer amplifier.

The anti-aliasing filter and the reset switch for the filter contribute kTC noise to the input signal of the ADC. This noise is due to the fluctuation of the remaining charge on the capacitor after it is reset and is directly related to the capacitor value. The formula for the reset noise is given by

Where k is Boltzmann’s constant, T is the temperature, and C is the value of the capacitor. In addition to reset noise, the RC filter contributes a voltage noise given by the formula

For the 5.6 nF capacitor, the kTC voltage noise is 0.86 µV and is uncorrelated for the two input filters. Even though this increases the noise contribution to the ADC to 1.22 µV, the voltage noise input to the ADC is negligible due to the RC filter.

The kTC reset noise for the filter is 30,000 e-. This reset noise translates to a voltage reset noise of 0.14 µV. Again, this reset noise is uncorrelated between the two filters which increases the reset noise input to the ADC to 0.20 µV and is a negligible contribution to the input noise to the ADC.

# Shutter Control

Each single board controller must provide a signal for the shutter control. This signal can be a TTL logic level which will drive an opto-isolator. The opto-isolator will connect to an external shutter controller and will provide isolation from any glitch, noise, or ground loop which may result from the shutter connection. A conceptual schematic is shown in Figure 9. When multiple cards must be used for a system, a single board will be chosen as the shutter master. Since all the cards in a system will be synchronous, any card can be chosen as the shutter master. The shutter signal must be actuated within an FPGA clock period of the shutter request and the shutter signal must remain high for the duration of the exposure. Thus, the shutter signal pulse must be able to remain high for a variable amount of time.

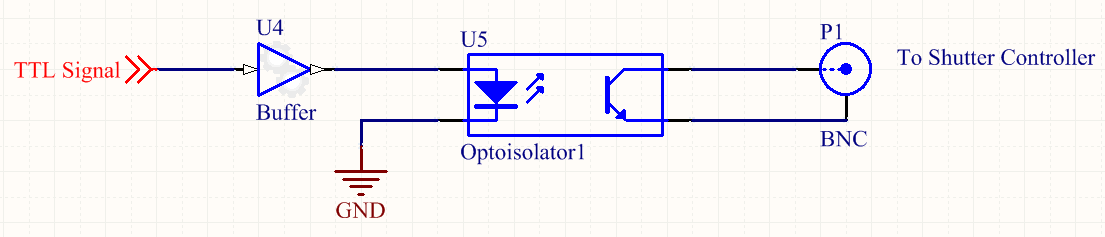


Figure 9: Shutter Control Concept

The host computer will initiate the exposure with a command to the single board controller along with a parameter for the duration of the exposure. The single board controller must be capable of sending back the elapsed time of the exposure to the host computer.

# Packaging

Each PCB will contain the resources necessary to run a single CCD. In the case of ZTF, these single board controllers will be packaged together in a chassis which will contain enough slots for 20 single board controllers and an additional 2 slots for power supplies. Connections to the CCD will be made from the back of the card, and the front of the card will have a single USB connection to a host computer. With this configuration, sliding a card out will only require disconnecting the USB cable. For WaSP, the configuration will be slightly different in that the single board controller will plug directly in to the VIB as shown in Figure 10. The same USB connection on the front of the board will be used to connect the card to the host computer.

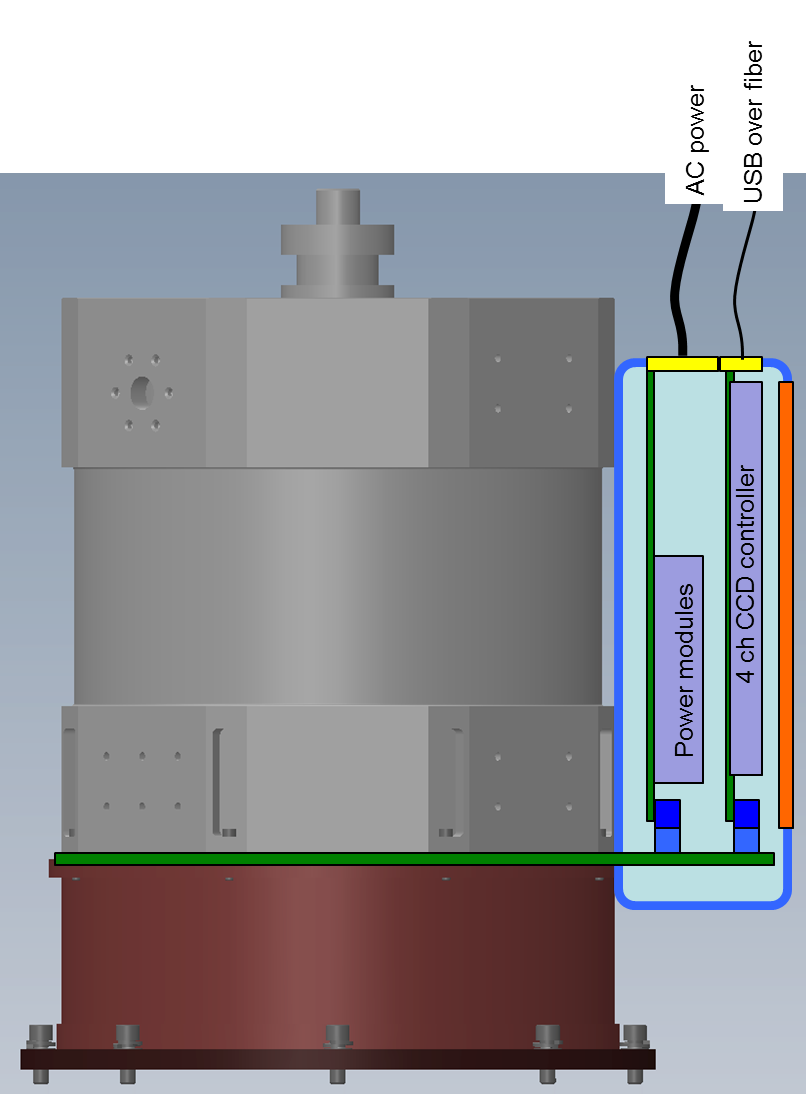


Figure 10: WaSP Board Packaging

The single board controller card will be a standard 6U sized eurocard. The dimensions of the card are 230 mm x 160 mm. The total card area for a single side is 36,800 mm2. With the present circuitry, a single board controller with 16 bias voltages plus one high voltage bias, 20 clock drivers, 4 analog signal chains, and a FPGA and USB driver will need an area of 29,175 mm2. The area calculator can be found at [this link](http://www.oir.caltech.edu/twiki_oir/bin/view/Palomar/ZTF/130718Electronics/ifpac_calc_simple_LMH6321_ON_OFF.xlsx) which shows the area requirements. The space needed for the circuitry is comfortably within the available space of the 6U card. Additional changes to the circuitry may change the space requirements, but the anticipated changes are on the order of 10%.

The board layout has three distinct sections to the board. The analog section contains the bias drivers and the analog signal chain. The clock section contains the clock drivers. The digital section contains the FPGA(s) and the USB serial link driver circuitry. Figure 11 shows a diagram of the board layout and the grounding sections of the board.

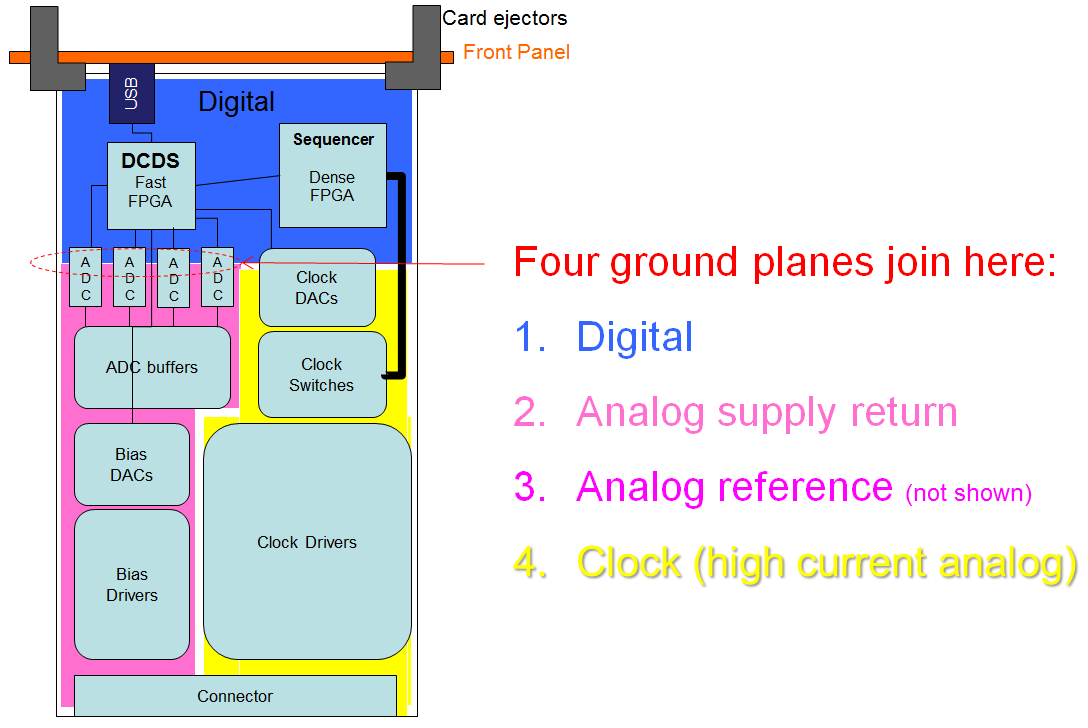


Figure 11: Single Board Layout

As shown in the grounding section, each of these areas on the board has their own ground plane.

On the front of the board are card ejectors and a front panel. The card ejectors are necessary for easy removal of cards from the chassis. An example of a good card ejector is a Schroff 60817-067. The mechanical design of the card must include mounting for card extractors. The front panel is necessary for mounting the USB connection. In addition to the USB front panel connection, there should be at least two more connections for the programmable digital output signals from the FPGA.

The back of the card has a section for connectors for the CCD. These connectors plug into a backplane which will provide power and route the CCD signals to the backplane. The single board controller design only requires a single digital signal, the synchronization signal, to be routed along the backplane as each controller card can function independently. The following tables show the signals which must be routed to the backplane for each single board controller. The tables are divided by bias, clock, and video signals.

Table 10 shows the pinout for the bias signals.

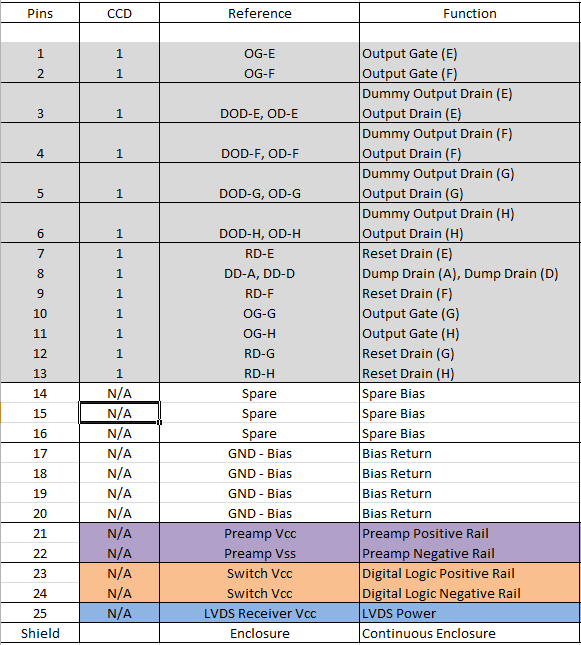


Table 11: Bias Pinout

The clock pinouts are shown in Table 11.

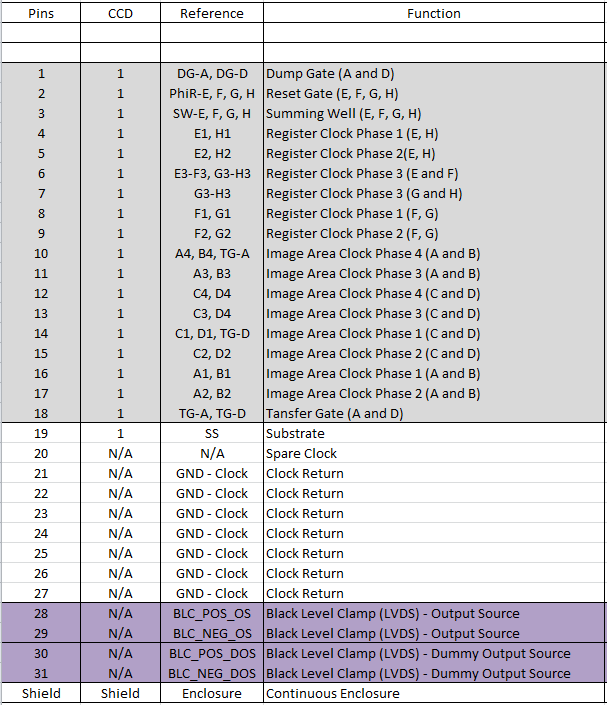


Table 12: Clock Pinout

The video signals are differential in nature and the routing of these signals must be made in differential pairs. The pinout for the video signals is shown in Table 12.

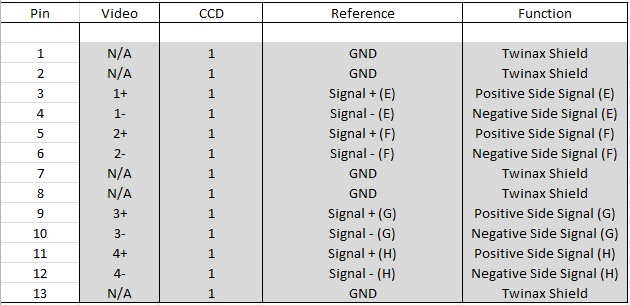


Table 13: Video Connector Pinout

FCI Metral connectors are recommended for the connection between the backplane and the single board controller card. The connectors can be found at [this link](http://portal.fciconnect.com/portal/page/portal/fciconnect/homepage).

The backplane connector for the power must accommodate the voltages shown in Table 6. These voltages may still be modified depending on final design but provide a good starting point.

The connection from the backplane to the instrument for ZTF is dictated by the cables and the available space on the VIB. The next section discusses the connections on the VIB and the associated cables.

# Cables to Controller

The cabling to and from the controller will be different for WaSP and ZTF. As described in other documents, for WaSP, the controller cards will plug directly in to the VIB board. This will require the same backplane connectors for the ZTF chassis will appear on the WaSP VIB board**. The pinout for these connectors is still to be determined depending on signal routing, power supply design, and potential test points. The connector and routing for the WaSP VIB will conform to the backplane connectors designed for the single board controllers. The WaSP interface has no other interface connectors.**

ZTF will use cables to transmit the signals to the VIB. A diagram of the connectors on the VIB is shown in Figure 12.

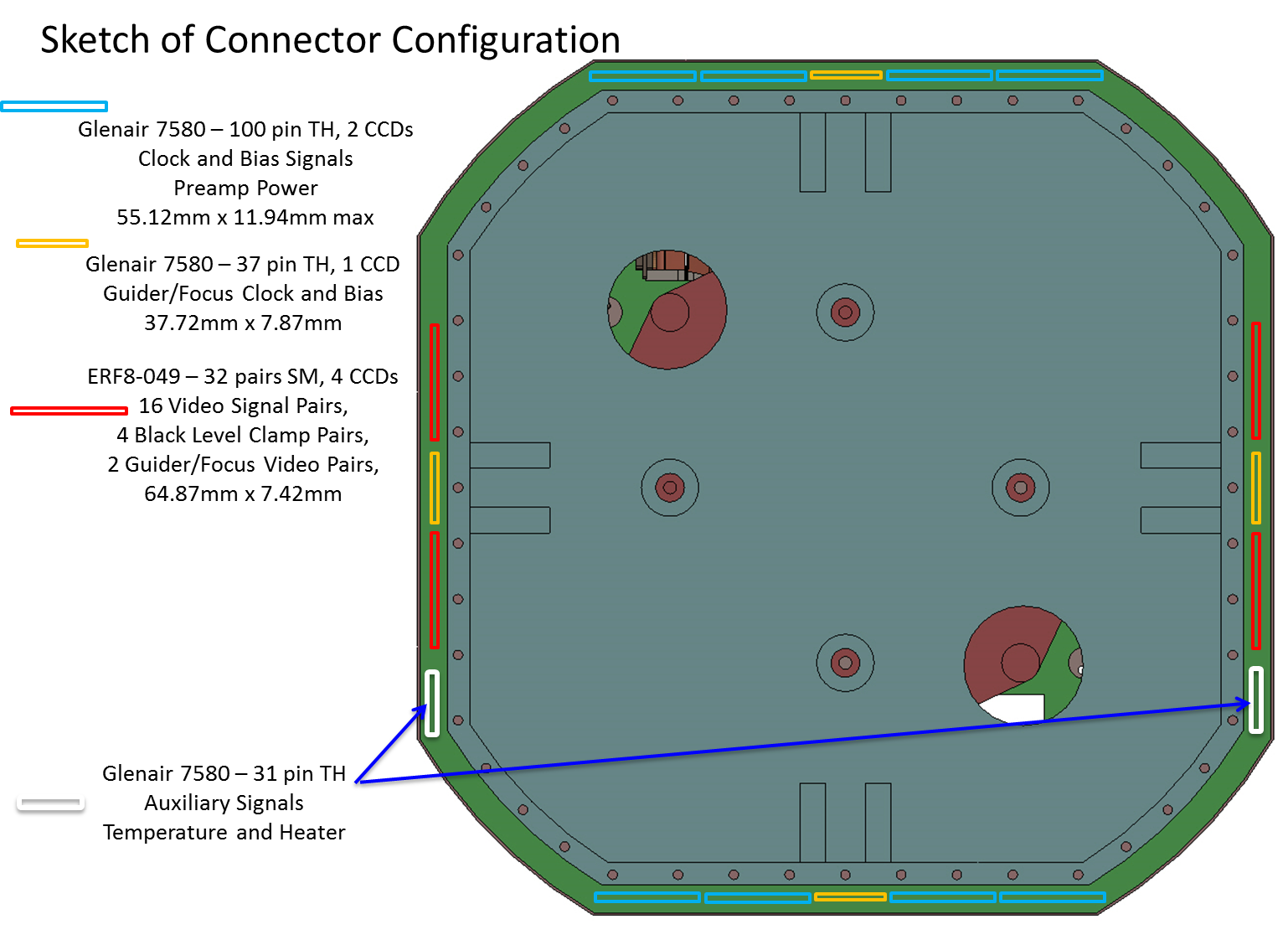


Figure 12: VIB Connector Layout

The clock and bias connectors and auxiliary signal connectors are manufactured by Glenair and can be found in the Glenair High-Performance Micro-D Connectors and Cables catalog. The 100 pin connectors for the science CCDs provide clocks and biases for 2 detectors. The 37 pin connectors for the guider and focus CCDs provide clocks and biases for a single focus or guider CCD. The 31 pin connector provides auxiliary signals for temperature control and monitoring and will not be routed to the single board controller cards.

The cables will be made by the connector manufacturer. The cables for the bias and clock signals will be a 177-710-2-100CS4K1-96MCG. The cables for the focus and guider clocks and biases will be a 177-710-2-37CS4K1-96MCG. The cables for the auxiliary signals will be 177-710-2-31CS4K1-96MCG. All cables are straight cables and have a 100% shield and ground spring. The ground spring will help to keep the shield continuous for the cables at the two connector ends.

The video signals are carried by cables manufactured by Samtec. These cables are a series of twinax cables which are formed into a flat ribbon cable. The twinax cable is a shielded twisted pair connection and will carry the differential video signals as well as a few LVDS signals for the preamplifiers on the VIB. The cable for the video connection is an ERDP-049 type cable.

The cable definitions have an implication for the connectors on the backplane which will route the signals to the VIB. **For every 5 controller cards there will be one Samtec connector, two 100 pin Glenair micro-D connectors, and one 37 pin Glenair micro-D connector. Due to a different connector for the guider and focus CCDs, there will need to be four slots which are reserved for boards to connect to the guider and focus CCDs.**

# Power Supplies

The power for the single board controllers will be provided by Vicor DC-DC converters with a front end AC-DC power converter. These power converters utilize a quasi-resonant ZCS/ZVS (zero current/zero voltage switch) topology. This topology allows for high power densities while reducing EMI and conducted noise. A typical ripple value for these supplies is ~100 mV and lower with increasing voltage. The micro DC-DC converters have typical power ratings of 75 W and 150 W in the small mini package.

The front end AC-DC power converter will be mounted at the side of the chassis and will accept 110 VAC power from the wall. The DC output of the converter will be routed to the power connector on the backplane which can then be used to power the power supply card. The power supply card will output the necessary DC voltages to the power connector to power the remaining single board controller cards.

The DC-DC power converters come in a mini package which measures 57.9 mm x 36.8 mm x 12.7 mm. The supplies will be mounted to a PCB card which will slide into the chassis and provide the power to the backplane of the chassis. In this way, the power supplies are modular and can be easily replaced by sliding in a spare power supply card. The package size will allow about 5 supplies to a card (230 mm X 160 mm) which will be just under the necessary number of supplies necessary. A two card system may need to be implemented.

Before a detailed design of the power can be made, a determination of the voltage and current requirements must be made. At this time, a reasonable listing of necessary voltages can be made and is found in Table 13.

|  |  |  |
| --- | --- | --- |
| Voltage | Function | Note |
| +36V | Analog voltage | Used to power bias voltage driver |
| +5 V | Analog voltage | Power for preamp, ADC buffer, bias DACs, and ADC |
| -5 V | Analog voltage | Power for preamp, ADC buffer, bias DACs, and ADC |
| +15 V | Clock voltage | Power clock driver |
| +5 V | Clock voltage | Power clock DACs and switches |
| -5 V | Clock Voltage | Power clock DACs and switches |
| +3.3 V | Digital Voltage | Power for FPGA(s) |

Table 14: Power Supply Requirements

Using typical power ratings for each voltage for standard Vicor AC-DC supplies, the deliverable current can be calculated and is shown in Table 14.

|  |  |  |
| --- | --- | --- |
| Voltage | Power | Current |
| +36 V | 150 W | 4.16 A |
| +5 V | 50 W | 10 A |
| -5 V | 50 W | 10 A |
| +15 V | 75 W | 5 A |
| +5 V | 50 W | 10 A |
| -5 V | 50 W | 10 A |
| +3.3 V | 50 W | 15 A |

Table 15: Power and Current of DC Supplies

At the present time, the current available for each voltage should be sufficient for 16 single board controllers.

For each of the supplies, the power and return pin of the supply will be routed to the power connector on the backplane. The return will be connected to the ground star point on each of the SBCs and the power will be routed to the appropriate section of the single board controller card. In this way, the return plane on any given card will be at a single potential, but the ground plane from card to card may vary slightly. A slight ground difference between cards will have minimal impact since all signal and data handling for a given CCD occurs on a single card. Refer to the next section in the document for more details of the grounding plan.

The chassis will have indicator LEDs which will indicated each power supply is within its specified voltage. These LEDs will come on at turn on of the chassis. When the controller cards in the chassis are programmed and initialized, the LEDs will be switched off for normal operation of the controller. This gives the user an indication that all voltages are correct and when the controllers are initialized. It also keeps the LED light from interfering with observation.

# Grounding scheme

The grounding scheme for the controller must be considered to enable a quiet design which will achieve desired performance. The grounding scheme must be planned on several levels – that is, on the board level, the cable level, and the system level.

The grounding at the board level involves the DC power supplies and the ground planes for each board. For each board, the proposed grounding is to have a digital ground, an analog supply ground, an analog reference, and a clock ground. The grounding scheme is shown in Figure 13.

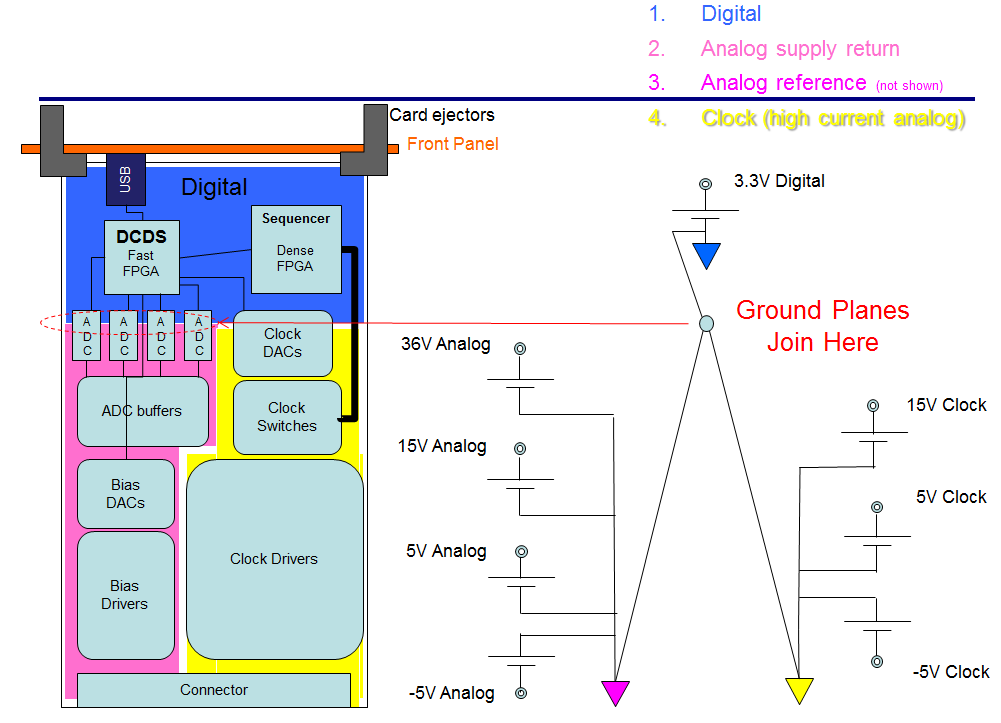


Figure 13: Grounding – Card Level

The supplies send both power and return along the backplane to each card in the chassis. Only at the single controller card’s star point are the returns for each power supply connected. Within each section of the controller card, there is a low resistance ground plane which will serve as a stable ground point for that section of the single board controller. This split of the ground planes has an effect on how the returns are supplied to the VIB.

The cable level grounding concerns the returns which are connected to the VIB for the preamp and the signals and returns supplied to the CCD itself. As mentioned earlier in this document, the substrate is driven by a voltage and the clock signals are capacitively coupled to the substrate. Therefore, the substrate bias is driven from the clock power supplies. A diagram of the situation is shown in Figure 14.

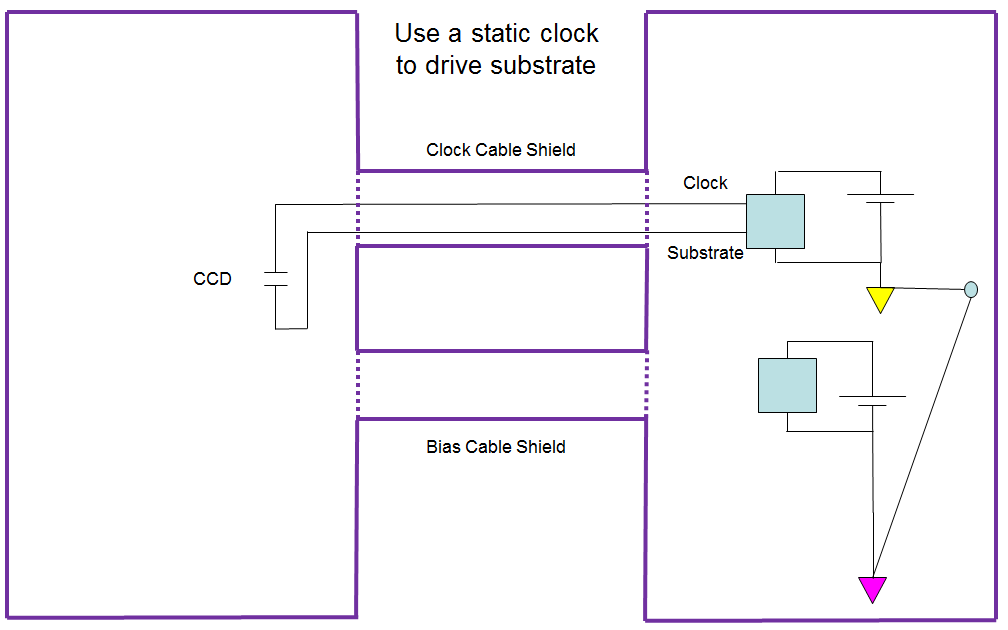


Figure 14: CCD Grounding – Cable Level

As shown in the diagram, the clock and substrate both have a return to the high current clock ground. The bias voltages and ground are not used for the substrate pin on the CCD.

The bias voltages and returns become important for the preamp circuit and the CCD’s output amplifier. Both of these are powered by bias voltages and analog voltages found in the analog section of the single board controller. A diagram of the analog voltage returns is shown in

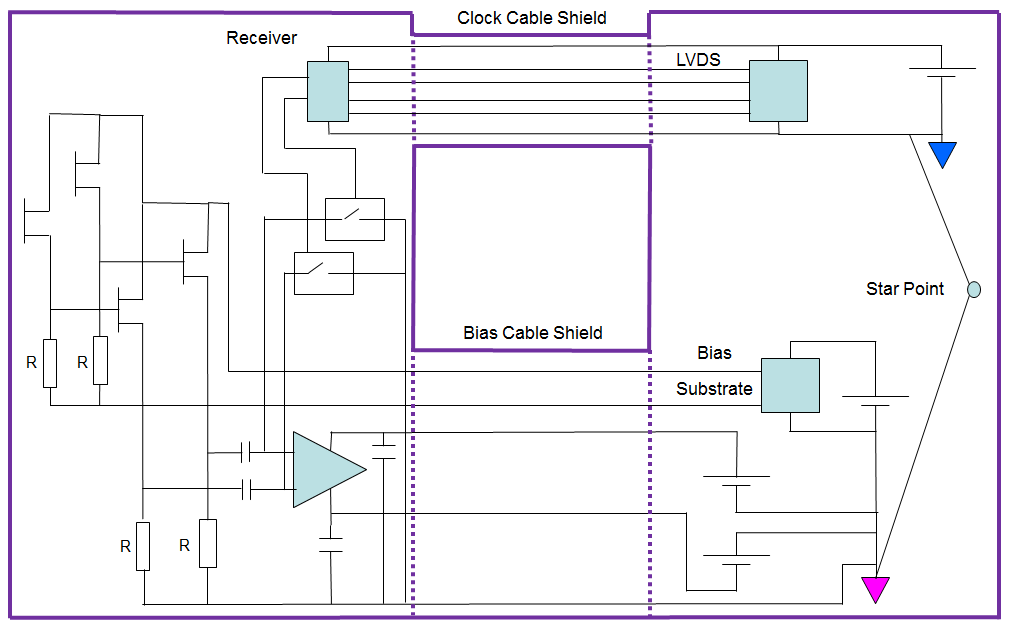


Figure 15: Bias and Preamp Grounding – Cable Level

Here, the bias provides the power to the CCD’s on-chip amplifiers. Also shown is the substrate connection to the first stage of the on-chip amplifier. A design question which must be investigated further is whether it is better to use the substrate voltage from the clock return or if the substrate voltage from the bias will result in a quieter output signal. The analog supply return is further used as the return for the amplifier load resistors and the preamp power supply filtering capacitors.

Note that in each of the above diagrams, there is a purple line encasing the controller chassis and dewar. The chassis and dewar are both encased in metal, and the shield of the cables is used to extend the enclosure through the whole system to keep out EMI. Unfortunately, there is little control over the grounding at the dewar side of the enclosure, but every effort will be made to keep a single point ground for the enclosure shield.

# Thermal Design and Requirements

The mechanical configuration of the two instruments drives the thermal requirements for the controller boards. In the case of WaSP, the controller board electronics is in the beam path and requires low power dissipation to the ambient air. For ZTF, the controller boards are mounted within chassis which will then dissipate the heat through a heat exchanger.

Since the instrument is in the beam path, an upper limit of 60 W dissipated to the ambient is placed on the electronics. For WaSP, the configuration uses three single board controllers. Each of the controller boards should dissipate no more than 20 W to the ambient air with a goal of 10 W.

A power dissipation calculator can be found at [this link](http://www.oir.caltech.edu/twiki_oir/bin/oops/Palomar/ZTF/130718Electronics/), which shows how dissipation is expected to scale with number of resources included within the controller. For 16 clocks, 20 biases and 4 video channels, the currently expected power dissipation is:

|  |  |  |  |
| --- | --- | --- | --- |
| Preamps | 1.6 | W | For four channels |
| Single board controller | 16 | W | Per board |
| Power supply | 2 | W | Average 90% efficiency |
| **Total per 4ch CCD** | **19.6** | **W** |  |

The layout of boards and power supply for WaSP is shown in Figure 16. This configuration allows the dewar to be used as a heat sink. Doing so will (more than) compensate for radiative and conductive cooling of the dewar walls by heat loss into the interior. The dewar wall temperature will be raised slightly above ambient temperature thus raising window temperature and reducing the risk of condensation. In WaSP the full demisting system includes venting dry boiloff gas in front of the window, after thermally equilibrating it to the dewar wall temperature. Thus the boiloff gas will compensate for (only) 2-3 W of controller power dissipation.

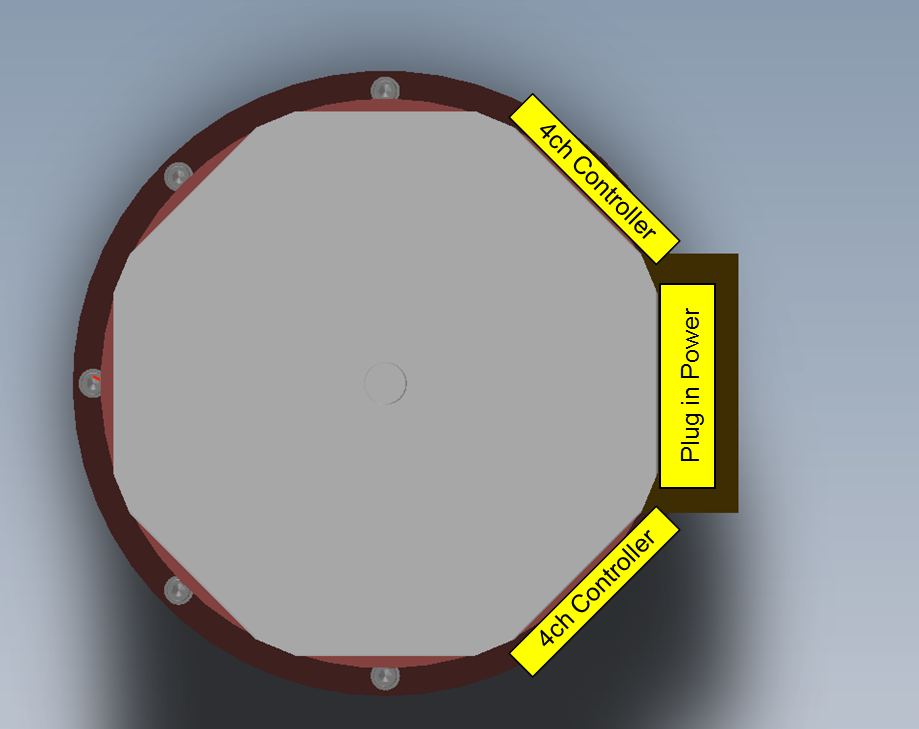


Figure 16: WaSP Configuration Top View

Rather than place air recirculation fans inside the narrow enclosures for the boards a more compact and efficient solution will be to use clamping card guides (called wedge locks) to provide good thermal contact between the chassis and cards. Eg.

http://www.wakefield-vette.com/products/accessories/wedgelocks.aspx



Figure 17: This wedge lock presses the card against the wall of a slot machined into the enclosure so that thermal contact is direct. In the process the card is secured against vibration.

The boards will be designed with isolated ground planes on the surfaces mating to the card guides these planes can increase the surface area for vertical thermal conduction to internal ground and power planes which provide the principal lateral conduction path.

# Host Computers and data handling

WaSP will have a single rack mounted Linux server acting as host. ZTF will use several such servers by distributing the data among multiple servers they can be relatively ordinary and inexpensive. Communication to/from the controller is over USB2 whose limiting through put is 480 MB/s per link. Each controller will send pixels as 32 bit signed integers more bits. For 4 channels per controller at 1MHz, this requires 128 Mbit/s plus framing bits, which is well below the USB2 capacity.

Tests will need to be performed to determine how many USB2 links can be serviced by one host at this rate. A factor of >3 reduction in data link speed can be achieved by buffering a full frame of data in the controller and transmitting during the subsequent exposure time. This may be required to reduce the number of host servers.

As a baseline, we suggest that four USB2 links (thus 4 CCDs) per server would be a good compromise so that the full 16 CCD mosaic would be handled by four science servers and one for guide and focus CCDs and supervisory software.

The 32 bit signed integers will be cached in memory then written as a set of compressed FITS files with one file per CCD. The FITS “tile compression” format will be used. This uses lossless Rice compression for the pixel data while not compressing the FITS headers. The image is divided into subarrays (tiles), which are compressed separately and many data reduction utilities are then able to uncompress only the part of the image being interrogated.

Compression during the initial disk write minimizes storage requirements, and avoids a penalty due to digital CDS producing data with more than 16 bit resolution. The first steps in data reduction usually result in conversion to signed 32 bit integers anyway and this numeric format allows us to dispense with the artificial offset needed to prevent noise and bias drifts from under-flowing a signed integer format.

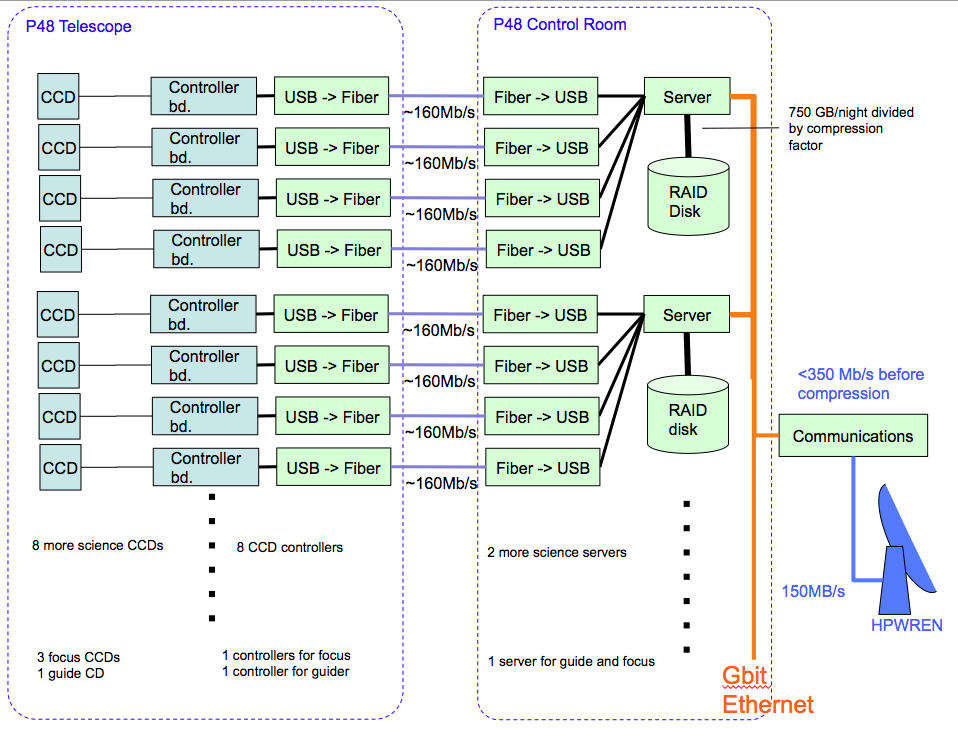
Images from the various CCDs are never aggregated into a single file per exposure. Instead, there will be one FITS file per CCD per exposure. We presume that the users will keep a data base to log exposures taken and the present location of the data. The file names will point to the origin of the data, thus

File name: ZTFxyUTyyyymmdd\_hhmmss

* + x = {1:4} (CCD position)
  + y = {1:4}

Using date and time to generate the file name avoids gap in sequence or duplicate names that can be caused by system crashes.

The servers and HPWREN (down link) will be connected by Gigabit Ethernet. Note that this downlink path is not shared with communication to the controllers.



**Data rate summary:**

* 1 Mpixel/s/ch
  + 4 ch/controller
  + 32 bits/pixel = 16 MByte/s = 128 Mbit/s raw data rate
  + \*10/8 = 160 Mbit/s per USB link (out of 480 Mb/s capacity)
* If four USB links per server, burst data rate = 64 MB/s/server.
* 9.5s read every 35s: average rate over exposure = 17.3 MB/s per server.
* Observing 12 hours per day at full efficiency (no long slews or other down time), average downlink rate = 17.3 MB/s \*12/24 \* 4 servers = 346 Mb/s. (Headers & telemetry assumed to be negligible overheads.)
* Lossless compression can to fit this into 150Mbit/s HPWREN throughput but not with much margin for other traffic. Some margin will come from twilight and down time, which has not been counted.

A current concern with the present FPGA is whether it can support the serial data rate produced by the ADCs. We suggest that it may be necessary to dedicate a smaller, faster FPGA to the signal path, providing both the digital CDS and USB2 interfaces. If data buffer memory is needed this would be an external RAM chip.

The “data FPGA” would delegate the Timing Generation, Clock and Bias DAC interfaces to a slower, higher density FPGA, which may have enough internal memory to store the tables defining the readout timing.

The data FPGA should also include a diagnostic mode to test the USB link. This diagnostic mode would consist of artificial data such as sequential numbers and will be writable at different speeds. A raw data mode is also required for the ADC. This raw data mode would transmit each conversion to the host computer.

# Diagnostics

Other diagnostics should be included on the single board controller. These diagnostics help to evaluate the state of health of the controller and, in some cases, the performance of the single board controller.

**The single board controller must provide a way to read back the parameters of the configuration. These parameters include bias voltage levels, clock rails, exposure timing, exposure time remaining as well as other parameters to be discussed.**

The single board controller should allow for an override to the black level clamp logic level. This override will allow the preamplifier to operate in single sided mode and in a shorted mode. The single sided mode will be helpful for diagnosing outside interference. A mode where both black level clamps are shorted will allow for a shorted input to the video processor.

Another useful diagnostic would be a slow input ramp to the video processor. A slow ramping input with the ADC sampling asynchronously at 1 MHz would produce a data set where any ADC value is equally likely. This data set can be used to measure the ADC’s differential non-linearity. If a slow input ramp can’t be generated on-board, use of flat illumination can produce the same data set. A goal would be to generate an on-board slow ramp so that this diagnostic would not require a CCD.