**Zwicky Transient Factory Camera- IFPAC Controller Qualification Plan: IUCAA Points**

**We shall need inputs from Caltech on following points by July end in order to check the feasibility of meeting January 2014 deadline for Generation 3.**

1. List of Additional Specifications required for Generation 3 Single Board Controller
2. Number of Clocks, number of serial and parallel clocks.
3. Maximum Capacitance for both Serial and Parallel Clocks after shorting CCD Pins if any.
4. Rise and Fall time requirement for Parallel and Serial Clocks, considering set up and hold time for DCDS and time available for Pixel transfer.
5. Voltage Rails for Clocks and whether clocks Uni, Bi or Tri-Polar.
6. Number of Bias Voltages
7. Driving current requirement for Bias Voltage
8. Voltage Rails for Bias Voltages
9. Type of Connectors on Single Board Controller
10. Connectors on Backplane side and Front side
11. Size of Card, constraint on either side
12. Backplane Card Size
13. Mechanical Drawings for Final Box, overall packaging details.
14. Type and numbers of Connectors Between controller box and Dewar
15. Cable length and type between Controller Box and Dewar.
16. PC Interface Specification: Hardware and Speed.
17. Acceptable Power Consumption for Single Board Controller.
18. Power Supply on Card: Can it be low noise Switch mode or Linear.
19. How many interfaces should the single board controller card have?

We have assumed one USB 2.0 as a default interface per card.

1. What kind of synchronization shall be required between different single board controllers?

Options:

1. Through Backplane with handshaking signals
2. With Dedicated communication card which can communicate with all single board controller cards over a fast Serial interface like RocktIO.
3. How many detectors are we going to control in total, should the system be scalable (at card or system level)?
4. What type of READ OUT modes and on board data processing (if any) shall be required?

e.g. Fast (beyond 1 MHz?) or slow clocking (ADC shall have limit on slower side also), channel swapping, Binning, ROI readouts, programmable or adjustable over scan and dark pixel regions, any other channel specific control

1. Do we need to have any on board memory for data storage / processing? If yes, how much?
2. What about shutter control and its interface.
3. Provision for test points – on board and at other places
4. Compatibility with WasP controller ? If specs for WasP are known then we can cross check.
5. We have assumed that each USB 2.0 interface shall be used to send data from only one detector to one Host PC.

Remember USB bandwidth is usually shared between peripherals and using multiple USB ports of a PC could end up in data loss. Host PC software shall extract the image information from data stream and after compression, etc create a FITS file (one per image / detector).

1. Full set of Specifications for Arbitrary waveform generation required

*Much of the above information on pints “r” to “aa” will help us in identifying and utilizing FPGA and its resources.*

1. Testing Requirement, Plan and Procedure Document considering new specifications for Generation 3, 4 and 5 Controllers.
2. List of Assumptions for Generation 3:
3. Single Board Controller controls One 4 channel CCD with Backplane architecture.
4. It uses 10 MSPS ADC ( AD7626)
5. 1 MSPS throughput per channel and DCDS with 5 pre and post reset samples.

May not have enough settling time.

1. Default USB 2.0 as a PC Interface per card.

**Also note following points related to delivery and your document:**

* Gen 1 and Gen 2 both can be delivered together by 1 Oct 2013
* Point 4 from ZTF IFPAC Qualification Plan Document dated 3rd July: Phased Qualification Plan detail: Generation I to Generation II will include laying out the electronics in the correct form factor for the final delivery of the controller.

*In above statement: Generation I and Generation II to be replaced with Generation III* and generation IV.