Meeting Notes July 11, 2013

Attendees: Stephen Kaye, Pravin Chordia, Mahesh Burse

**Minutes**

* Discussed phased delivery schedule. IUCAA has discussed it in the lab and will send out a document detailing what work they think they can do in the time allotted
* Document about phased delivery will be sent today or Monday
* Test results for using LM7171 as the driver were posted and discussed
* Rise time is acceptable for serial clocks for up to 680 pF capacitive load for a 10V swing. This puts an upper limit on number of phases which can be ganged
* The power savings from using the LM7171 and eliminating the LMH6321 was discussed. Approximately 10W is saved eliminating the LMH6321
* Tri-level clocks were discussed. The tri-level clocks cause an increased complexity when using the present clock driver circuit
* A different clock driver circuit will need to be implemented for tri-level clocks
* Preliminary schematics for the DCDS signal chain was posted. A more in depth review of the schematics will take place over the week

**Action Items**

**IUCAA**

* + Send document concerning delivery schedule
  + Review document on tri-level clock scheme

**Caltech**

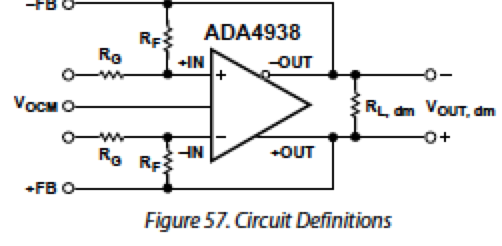
* + Review clock ganging to make sure capacitance values are below ~680pF for any serial clock
  + Send IUCAA information about tri-level clock scheme and recovering charge from traps

## Further comments by Roger:

Since I was unable to dial in, I am supplying some comments here…

### DCDS schematic.

As a matter of principal I think we should not show a rectangular symbol for a multiple op amp IC even if it has a special configuration as a differential ADC driver. The rectangle tells us nothing about the internal function. Can we use a symbol that looks like the one offered by Analog devices in their data sheet, please. i.e.



Steve or Pravin, can you remind me why we need two offset DACs.

In fact do we actually need any offset DAC? Could we get away with a fixed offset ?

What is the DAC output drive capability ? Do we really need a buffer for the offset voltages? I see that R102 is only 50 ohms. Why such a low resistance?

The offset voltage DACs consume 150 mW each and will get quite hot (15mA with +-5V supplies). They have very high bandwidth and very low noise, which seem unnecessarily aggressive.

At maximum output (5V) the 50 ohm load resistors (R792 and R32) would draw 100 mA. Why are you loading down the DAC so much. The short circuit current is 30mA so this wont work anyway.

Why does the offset buffer have a gain of 2?

## Power consumption spreadsheet

This is looking much better now!

## Settling time for capacitive loads spreadsheet

I am quite happy with the LM7171 performance without the LM6321 buffer. The slew rate is good and the edges look clean. The space and power savings are higher priority than the added drive current.

We need to turn our attention to the DAC and timing generator specs.

-- Roger