Meeting Notes June 27, 2013

Attendees: Stephen Kaye, Pravin Chordia

**Minutes**

* Discussed reducing power by eliminating MOSFET driver (LMH6321)
* Pravin did tests with the driver removed and LM7171 driving 470pF and 680pF loads
* Rise time increased from ~14ns to 50ns when using just the LM7171 driver
* Quiescent current dropped from 410mA to 250mA. Saving 160mA from +/-15V quiescent.
* Supply current increased to 300 mA while driving the load, but a similar increase was not observed when the MOSFET driver was used to drive the load.
* Post test results to twiki (Action for Pravin)
* Discussed rise time and drive current calculations for the clocks.
* Pravin noted that the rise time for the register clocks may be too slow. CDS operations take time and a faster clock may be needed.
* Revisit timing diagram including the rise time for the clocks and DCDS (Action for Steve)
* Discussed using unipolar clocks and driving the Vss
* Look at power savings with unipolar clocks (Action for Pravin)
* Discussed tri-level clocking for increased CTE
* Need to investigate impact of new clocking scheme. Both IUCAA and Caltech will study.
* Preliminary schematic of digital CDS signal chain is complete. Pravin will post to twiki

**Action Items**

**IUCAA**

* + Post results of test with LM7171 driving capacitive loads
  + Calculate power savings from using unipolar clocks and driving Vss
  + Think about tri-level clocking scheme
  + Post preliminary schematics for DCDS signal chain

**Caltech**

* + Review timing diagram for DCDS with special attention to register clock rise times
  + Think about tri-level clocking scheme
  + Finish and post connection scheme for SBC to determine board area requirement