Meeting Notes June 20, 2013

Attendees: Stephen Kaye, Pravin Chordia, Roger Smith

**Minutes**

* Discussed the latest power and area spreadsheet
* Spreadsheet is for 16 clocks which is what is needed for 1 CCD. But spare clocks are a good idea and we will move this up to 20 clocks (5 banks of 4)
* In addition to and extra bank of clocks, a bank of 4 LVDS signals are needed for functions on the VIB. These signals will be provided directly from the FPGA
* The controller pinouts spreadsheet needs to be reviewed for the low clock rail and the substrate voltage. +/-10V will be necessary with substrate held to ground (Action for Steve)
* An attempt will be made at reducing the power necessary for the clock drivers. Ideas put forth – lower drive current (eliminate mosfet driver), disable clock driver when not needed, reduce op-amp supply voltage if op-amp is rail-to-rail. (Action for Pravin)
* Examine necessary rise times and current needs for the CCD phases (Action for Steve)
* Board shape and size is still an open issue. Board edge connectors need to be defined and the system connections need to be defined. This will set a board size requirement. (Action for Steve)
* Mahesh is working on waveform generation document and host computer interface document. The documents should give a big picture idea of the interfaces. Will be posted soon. (Action for Mahesh)
* After documentation, clock driver and backplane are in a state where they can be sent for a test/demonstration
* Effort will be switched from testing the analog CDS circuit toward the new signal chain implementation (DCDS)
* A document describing the digital CDS will be started (Action for Roger)
* A document describing the preamps will be started (Action for Roger)
* A document to start the conversation about built-in diagnostics will be started (Action for Roger)

**Action Items**

**IUCAA**

* + Look over op-amp options for the clock driver circuits to reduce power consumption
  + Continue work on waveform and interface documents

**Caltech**

* + Review clock levels with respect to the substrate voltage
  + Review current drive needs for the clock phases
  + Define connection scheme to determine board area requirement
  + Begin writing documents on the preamp, DCDS, and built-in diagnostics