Meeting Notes June 6, 2013

Attendees: Stephen Kaye, Pravin Chordia

**Minutes**

* Discussed power calculations for the various boards
* Current numbers are from data sheets
* Power calculations are to run a single CCD
* There is some question as to whether the current figure is from Vcc to ground and Vss to ground or between Vcc and Vss
* IUCAA will further look at current specifications for the ICs
* Current for +5V is quite high. USB driver and SFP (Ethernet fiber Tx/Rx) are power hungry
* Board area was discussed and was based on a single board controller for a single CCD
* Bias circuit is in a group of 4 (quad DAC)
* Clock circuit is in a group of 4 (octal DAC and two DAC channels to run a clock)
* Feedthroughs are the filters that are used for the backplane card and may not be necessary for SBC
* Area calculated from laying out present clock and bias circuits
* Single board controller will fit on a 6U card
* Discussed measured currents from clock driver card
* Agreed fairly well with calculated currents
* A new power supply was used which could run 15 clocks. The old power supplies could not source the necessary current.
* To leave a clock channel idle, the resistor between the FPGA and clock switch was removed.
* Current for 5V is only 377mA. Adding the USB driver and SFP increase the current to the calculated 865mA
* Discussed schedule and deliverables. The waveform generation document and host interface document milestones are approaching.
* We will be more prepared to discuss schedule when Mahesh and Ram return

**Action Items**

**IUCAA**

* + Double check the currents in the calculated power spreadsheet
  + Continue work on waveform and interface documents

**Caltech**

* + Create document concerning schedule and sharing of prototypes for testing