**IFPAC Options**

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|  | **Two Card System** | **Single Card System** | | | |
|  |  | Option 1 | | Option 2 | **Remarks** |
| Analog Channels | **8** | **8** | | **4** |  |
| Clock Drivers | **31** (15 + 15 + 1 EMCCD) | **31** (15 + 15 + 1 High Voltage) | | **16 or More?** |  |
| Bias | **24** | **24** | | **12 or More?** |  |
| FPGA | **2** | **1** | **2** | **1** |  |
| USB Interface | **1** | **1** | **1 or 2** | **1** |  |
| Size | **2 Cards 100 \* 240 mm**  ( Will require about **50 sq mm** more area on Analog Card **for Bias generation**) | **233 \* 220 mm Standard 6U Card** (May be very tight, length 220 mm may have to be increased**)** | **233 \* 220 mm Standard 6U Card** (May be very tight, length 220 mm may have to be increased**)** | **233 \* 160 mm Standard 6U Card,** It may also takeRFI/LC Filtering. |  |
| Pros | This system if used for 1 CCD can almost drive any CCD in all modes. | Most of the existing FPGA code can be used. | Resources between two FPGAs could be shared | Most of the existing FPGA code can be used. |  |
| Cons | If clocks are not sufficient for 2 CCDs, 4 Analog Channels will not get used. | If clocks are not sufficient for 2 CCDs, 4 Analog Channels will not get used. | If clocks are not sufficient for 2 CCDs, 4 Analog Channels will not get used. | We can increase number of Clocks and Biases, may be required for One ZTF CCD |  |
| High Speed ADC Data has to travel from one card to another via Backplane | Routing this single Board may be very complex. | New FPGA code will have to be written.  . |  |  |
| Note | **Area required for LC Filtering on Backplane not considered.** | | | |  |
| **Out of 24 Biases 16 nos. will be 0-25 V and 8 nos. will be +/-13V.**  **Out of 12 Biases 8 nos. will be 0-25 V and 4 nos. will be +/-13V.** | | | |  |