**Power Supply Requirement for IFPAC –**

**1 CCD, 4 Channel Analog Processing and 15 Clocks**

**Quiscent Current Calculatons**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Clock Driver Card 15 Clocks** | | | | | **Analog Card 4 Channels** | | | |
| DAC AD8842 | MUX | LM7171 | LMH6321 | FPGA + Interfaces | Analog Processing Amlifiers | ADC | Bias 4 nos. | Bias 8 nos. |
| +/-5.5 V | +/- 5.5 V | +/-15 V | +/-15 V | +5 V + USB ? | *+/-5.5.V* | *+5 V derived from +/-5.5V* | *+/- 15 V* |  |
| 15 mA each Power \* 4 | 8 mA \* 15 | 9.5 mA \* 15 | 20 mA \* 16 | 1.5 A |  |  |  |  |
| 60 mA | 130 mA | 150 mA | 320 mA |  |  |  |  |  |
|  |  | Total Quiescent Current without load = 470 mA | |  |  |  |  |  |
|  |  |  | |  |  |  |  |  |
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|  |  |  | |  |  |  |  |  |

**Measured**

**Power Supply Currents Measurement For Clock Driver Card without Load**

1. +5V     :  400 mA

Used to Power Digital Section i.e. FPGA. Load is close to quiescent as only firmware running is 15 clocks generated by FPGA.

1. +15V /- 15 V ~ 400 mA each i.e. total 800 mA into GND

This power is used for Gain Amplifier and Buffer i.e. Driver Amplifier. All the 30 Channels are powered and 15 Clocks running without Capacitive Load. This is close to quiescent current.

1. +/- 5.5V ~ 375 mA each i.e. total 750 mA in GND.

All DACs runs on this power supply. All DACs are powered and half of them are generating DAC voltages driving gain stage.

**Power Supply Currents Measurement for Clock Driver Card with Load**

FPGA hardly has any code in to it. Power is close to quiescent power consumption. No PC Interfaces, USB, fiber interface active.

Four phase shifted Clocks running at 1 Mhz driving in to 300 pF Load

Four Phase Shifted Clocks running at 40 KHz driving 47 nF

Two Phase Shifted Clocks running at 20 KHz driving 47 nF

Five Phase Shifted Clocks running at 10 KHz driving 47 nF

+5V   =  700 mA (FPGA Power)  
+15V  =  526 mA  
-15V  = -534 mA  
+5.5V =  384 mA  
-5.5V = -324 mA