Meeting Notes May 23, 2013

Attendees: Stephen Kaye, Roger Smith, Pravin Chordia, Mahesh Burse

**Minutes**

* Discussed board area and 4 channel versus 8 channel SBC
* Options presented are for a 6U card
* Some savings in area occur due to simplified signal chain
* Single FPGA architecture preferred due to reusable code
* 3U card was suggested for a 4 channel card
* ADCs need to be near FPGA which works better in 4 channel board
* All will think more on 4ch vs. 8ch board and board area
* Number of biases and clocks need to be revisited for each configuration
* Ganging of clocks causes different capacitive loads – needs to be investigated
* ADC running at 10 MHz is ok, but 166 MHz bit clock cannot be supported now
* 166 MHz clock for echoed-clock mode – other mode requires higher clock rate.
* Present design does not have enough pins for this mode
* A reduced pin demand allows for echo-clocked mode
* Internal frequency generation for FPGA will be investigated
* Need to create a block diagram of data handling within FPGA
* Concerns over 32 bit data and speed of USB driver chip
* Output drain biases see crosstalk when they are connected together. Need to rethink bias ganging
* Clock card power reviewed. More measurements will be made this week.

**Action Items**

**IUCAA**

* + Measure power for clock board with no clocks running, 1 clock running, 2 clocks running… Put measurements in spreadsheet
	+ Update board area for 4 channel board with DCDS. Put in spreadsheet with board area for each clock, etc.
	+ Investigate internal clock speed possible for FPGA

 **Caltech**

* + Re-visit the clock and bias requirements for CCDs. Calculate capacitive loads for clocks.
	+ Create block diagram of data processing within FPGA