Meeting Notes May 16, 2013

Attendees: Stephen Kaye, Roger Smith, Pravin Chordia, Mahesh Burse

**Minutes**

* Single card controller (SCC) was focus of meeting
* Advantages/challenges for SCC were presented
* Multiple SCCs need to be synchronized.
* Shutter will need to be generated.
* If generated from the clock FPGA on each SCC, the multi-SCC systems have redundant shutter signal
* If generated separately, it needs to be synchronized with the clocks
* Board area for SCC is an open question at this time
* Power supply need for SCC is an open question
* Timing diagram for ADC was discussed
* Is dead time necessary between data bursts?
* Timing diagram needs to be annotated – will be re-worked and re-posted
* We need to gather information about a 4 channel SCC vs. 8 channel CCD
* IUCAA will take another look at the server configuration information

**Action Items**

**IUCAA**

* + Estimate board area requirement for 4 channel and 8 channel SCC
  + Estimate power consumption per power supply for SCC (4ch vs. 8ch)
  + Provide guidance on FPGA speed versus FPGA resources used – do we separate the clock timing and ADC FPGAs? Is the answer different for 4ch vs. 8ch SCC?

**Caltech**

* + Re-visit the clock and bias requirements for CCDs with an eye toward 4ch vs. 8ch SCC
  + Annotate and re-work timing diagram
  + Make diagram of data flow – include data formats and data speeds at points along flow
  + Create drawing of ground plane concept for SCC