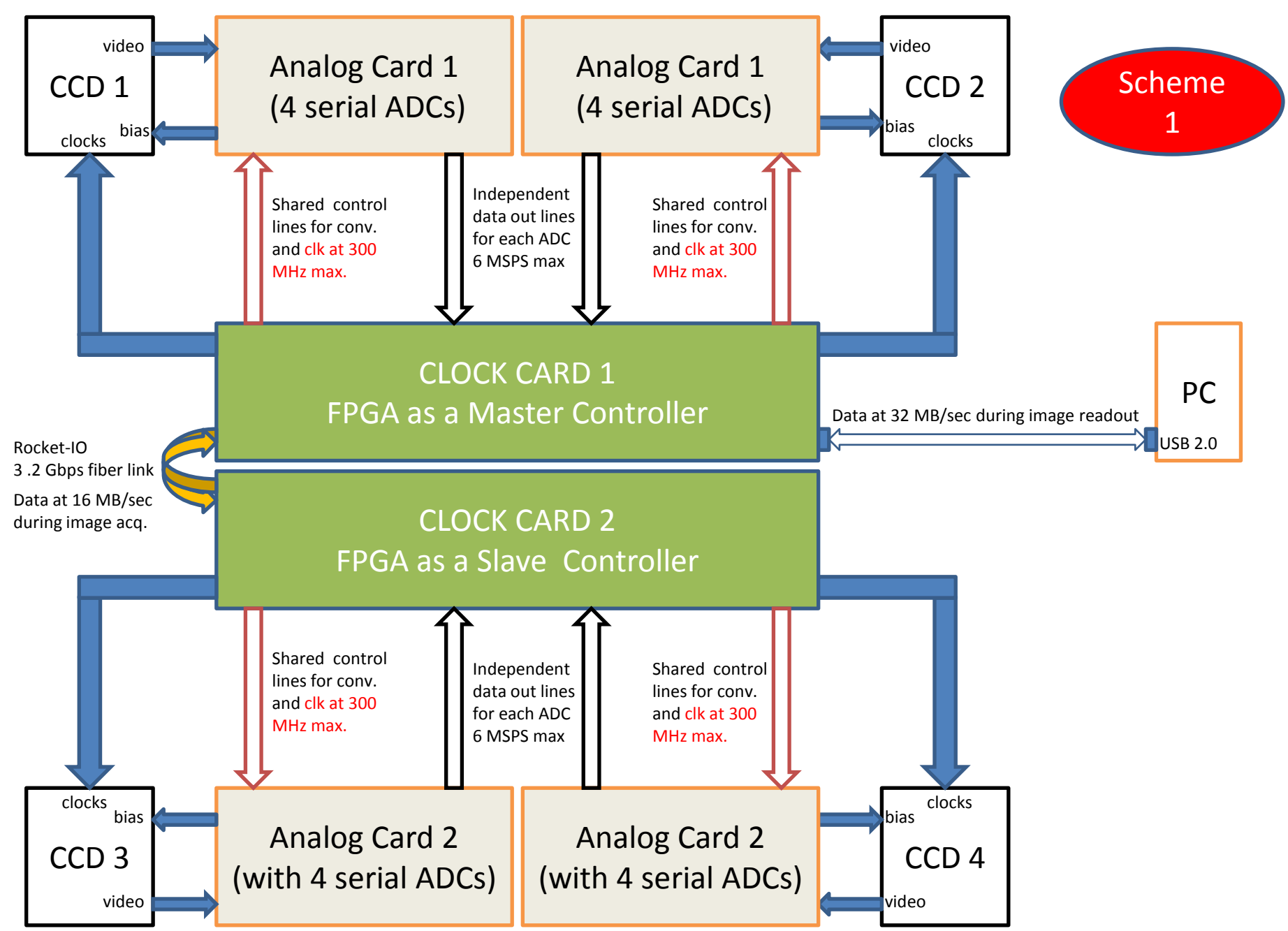
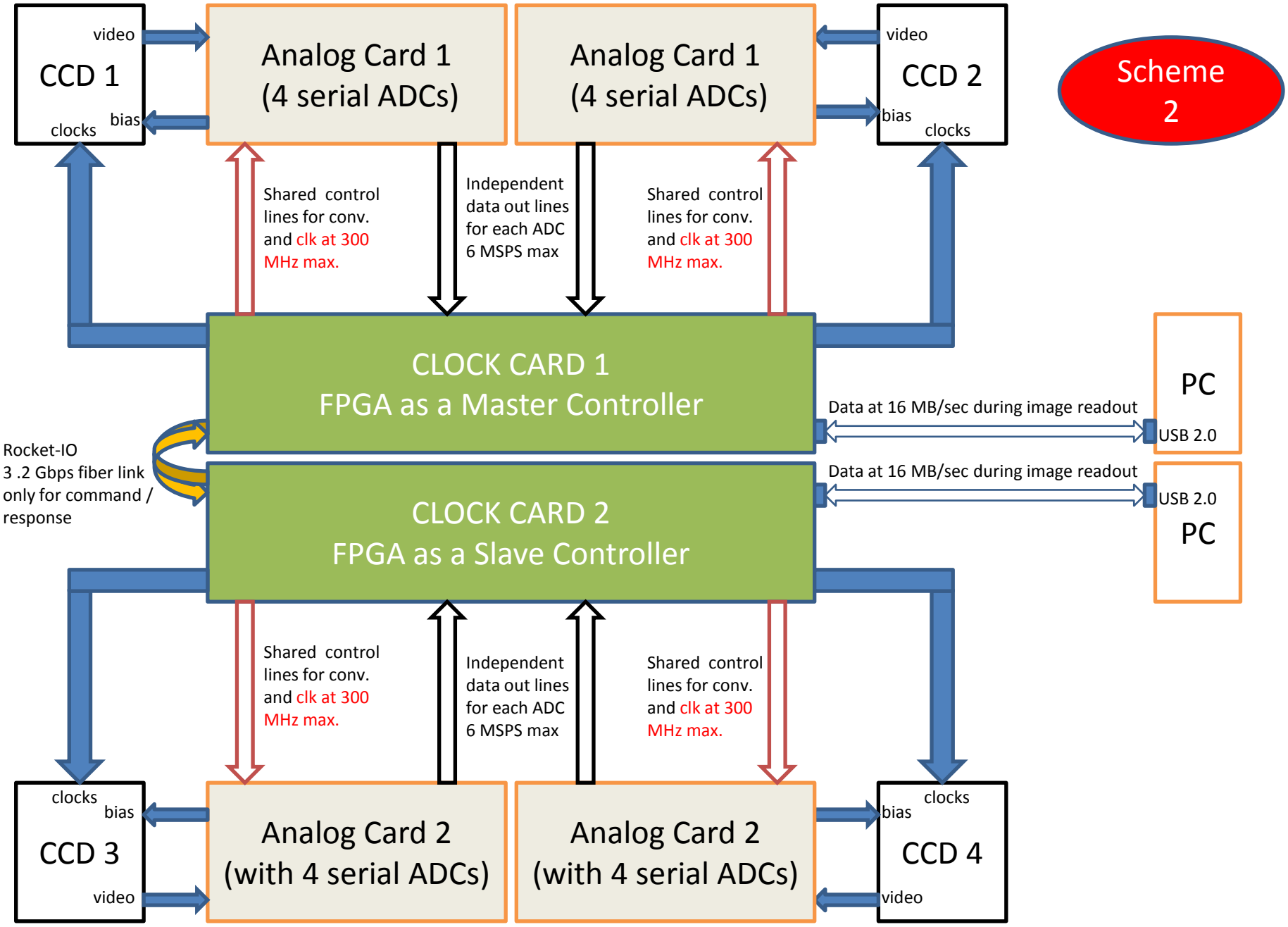
Scheme 1

- One USB interface to handle 4 CCDs
- 4 host computers shall be required for ZTFC (16 CCDs)
- Each FPGA reads data from 8 ADCs and performs DCDS
- Maximum data throughput rate would be 32 MBytes / sec per interface
- Reading ADCs at 300 MHz clock is going to be a challenge (current code uses 100 MHz clock).


Scheme 1
CCD 1
video
clocks
bias
CCD 2
video
bias
clocks
Analog Card 1 (4 serial ADCs)
Analog Card 1 (4 serial ADCs)
Shared control lines for conv. and clk at 300 MHz max.
Independent data out lines for each ADC 6 MSPS max
Shared control lines for conv. and clk at 300 MHz max.
CLOCK CARD 1
FPGA as a Master Controller
PC
Data at 32 MB/sec during image readout
USB 2.0
Rocket-IO
3 .2 Gbps fiber link
Data at 16 MB/sec during image acq.
CLOCK CARD 2
FPGA as a Slave Controller
Shared control lines for conv. and clk at 300 MHz max.
Independent data out lines for each ADC 6 MSPS max
Shared control lines for conv. and clk at 300 MHz max.
CCD 3
clocks
bias
video
CCD 4
clocks
bias
video
Analog Card 2 (with 4 serial ADCs)
Analog Card 2 (with 4 serial ADCs)

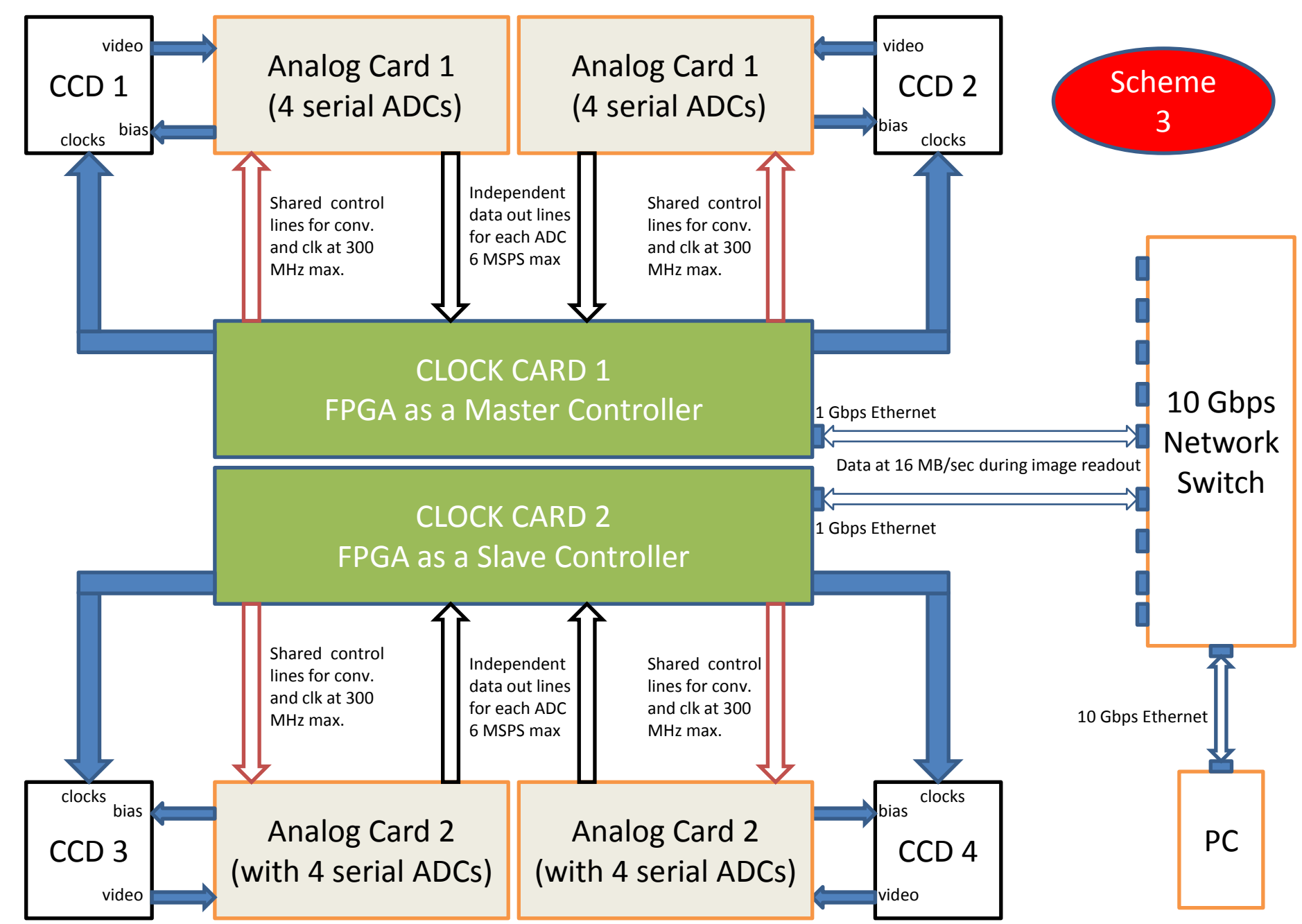
Scheme 2

- One USB to handle all commands for 4 CCDs plus image data readout from 8 ADCs (2 CCDs)
- Other USB only for image data acquisition from 8 ADCs (2 CCDs)
- 8 host computers shall be required for ZTFC (16 CCDs)
- Each FPGA reads data from 8 ADCs and performs DCDS
- Maximum data throughput rate would be 16 MBytes/sec per interface
- Reading ADCs at 300 MHz clock is going to be a challenge (current code uses 100 MHz clock).


CCD 1
video
clocks
bias
Analog Card 1
(4 serial ADCs)
Analog Card 1
(4 serial ADCs)
video
CCD 2
bias
clocks
Scheme
2
Shared control
lines for conv.
and clk at 300
MHz max.
Independent
data out lines
for each ADC
6 MSPS max
Shared control
lines for conv.
and clk at 300
MHz max.
CLOCK CARD 1
FPGA as a Master Controller
PC
Data at 16 MB/sec during image readout
USB 2.0
Rocket-IO
3 .2 Gbps fiber link
only for command /
response
Data at 16 MB/sec during image readout
CLOCK CARD 2
FPGA as a Slave Controller
USB 2.0
PC
Shared control
lines for conv.
and clk at 300
MHz max.
Independent
data out lines
for each ADC
6 MSPS max
Shared control
lines for conv.
and clk at 300
MHz max.
clocks
bias
CCD 3
video
Analog Card 2
(with 4 serial ADCs)
Analog Card 2
(with 4 serial ADCs)
clocks
bias
CCD 4
video

Scheme 3

- 1 Gbps Ethernet link per clock card
- Each clock card to read 8 ADCs (2 CCDs) and perform DCDS
- 16 links would be required for ZTFC
- All links can be terminated into 10 Gbps network switch
- Reading ADCs at 300 MHz clock is going to be a challenge (current code uses 100 MHz clock).
- Present clock card can support only UDP, due to this data packets could be lost due to busy network or for other reasons


Scheme 3
CCD 1
video
clocks
bias
Analog Card 1 (4 serial ADCs)
Analog Card 1 (4 serial ADCs)
CCD 2
video
bias
clocks
Shared control lines for conv. and clk at 300 MHz max.
Independent data out lines for each ADC 6 MSPS max
Shared control lines for conv. and clk at 300 MHz max.
CLOCK CARD 1
FPGA as a Master Controller
1 Gbps Ethernet
Data at 16 MB/sec during image readout
CLOCK CARD 2
FPGA as a Slave Controller
1 Gbps Ethernet
10 Gbps Network Switch
Shared control lines for conv. and clk at 300 MHz max.
Independent data out lines for each ADC 6 MSPS max
Shared control lines for conv. and clk at 300 MHz max.
10 Gbps Ethernet
CCD 3
clocks
bias
video
Analog Card 2 (with 4 serial ADCs)
Analog Card 2 (with 4 serial ADCs)
CCD 4
clocks
bias
video
PC