Meeting Notes May 9, 2013

Attendees: Stephen Kaye, Pravin Chordia, Mahesh Burse

**Minutes**

* Bias loading test results were discussed.
* Frequency compensation circuit topology was corrected to the configuration in the design note and the results still had a spike
* Suggestions that it is the output impedance of the op-amp were raised
* MOSFET switching was also questioned. The MOSTFET was previously tested on its own power supply and did not exhibit the spike which is seen with these tests.
* IUCAA presented the data flow schemes for the controller
* The ADC clock needs to run at 300 MHz (!) which might not be possible with the FPGA
* Scheme 2 from IUCAA handles 8 ADC channels/host computer
* Two clock/analog board pairs are synchronized, but further synchronization is not possible at this time
* Ethernet link has been tested, but there are lost packets
* Caltech server configurations were discussed
* Presently, only 2 clock cards can be synchronized. To synchronize more cards, a ‘super master’ clock card needs to be designed
* Presently, scaling the system needs extra design in the ‘super master’ clock card
* Synchronization of all clock cards is necessary
* Red Hat Enterprise Linux is used at IUCAA, this may be made the operating system for the controller
* The testing and deliverables were discussed
* There are multiple sets of boards, and the extras can be delivered to Caltech
* The digital CDS may need a quickly designed new analog board. Steve thinks this is unnecessary, and it will be discussed offline

**Action Items**

**IUCAA**

* + Will do further tests on bias loading and discussions on source of spike
  + Think about synchronizing multiple cards
  + Further discuss ADC clock rate and digital CDS testing

**Caltech**

* + Investigate ADC clock requirements
  + Discuss/recommend tests for bias loading spikes
  + Detail how digital CDS test configuration
  + Detail preamp signal test configuration