Meeting Notes May 2, 2013

Attendees: Stephen Kaye, Roger Smith, Pravin Chordia, Mahesh Burse

**Minutes**

* Bias loading test results were discussed.
* The frequency compensation circuit topology is different than the classic in-the-loop compensation. A design note was sent out to all featuring the compensation circuit
* IUCAA will draw up the new circuit and test it with various capacitive loads
* The bias and clock cards are partially done, but the power supply current is still an issue
* Current theory: In-rush current is too large for the current power supply
* Another power supply is on order to use for the bias and clock cards
* While waiting for the power supply, a power calculation for the cards will be done. This will be compared to present loading of the power supply
* The data throughput conversation was started.
* The recommendation is that there are parallel data paths to multiple host computers
* Multiple host computer configurations will be explored and discussed with the scientists
* Some clarity is needed for the data path within the controller. How does data flow from multiple ADCs to the clock FPGA and then from the FPGA to the computer
* A diagram will be drawn up showing the controller data path

**Action Items**

**IUCAA**

* + Will do further tests on bias loading after the compensation circuit is changed
  + Do a calculation for expected current draw for clock, analog, and backplane boards
  + Draw up a diagram detailing the data path within the controller

**Caltech**

* + Will explore the host computer configurations for the data logging
  + Complete a discussion on deliverables and goals for tests for the delivered items