Meeting Notes April 25,2013

Attendees: Stephen Kaye, Roger Smith, Pravin Chordia, Mahesh Burse

**Minutes**

* Bias loading test results were discussed.
* A large transient appears when the load current is turned off. Roger thinks this is due to the inductor (ferrite bead).
* A slope occurs on bias voltage when op-amp is powered by +30V. This will be investigated.
* 100 mV of high frequency noise appears on signal.
* Changing the connection of the test probe was recommended
* Other methods of reading bias voltage noise recommended such as capacitively coupling bias signal to analog signal input and taking ADC data.
* It was recommended to write up the test results into a document. Test document should include description of test, why test is being done, and what the results are
* Power point document can be used to show pictures along with arrows and words to describe test and test results.
* Schedule was briefly talked about. A description what what is completed on the clock and analog boards was requested
* ADC data throughput was discussed. Caltech will provide a write up of further questions.
* The system interconnections was presented

**Action Items**

**IUCAA**

* + Will do further tests on bias loading
    - Testing with the inductor shorted
    - Try different bandwidth settings on oscilloscope to see what is happening with the lower frequencies
    - Try adjusting the connection of test probe (e.g. shorter probe ground lead, etc.)
  + Write up of further test results
  + A description of what is completed on each of the analog and clock boards

**Caltech**

* + Will write up questions concerning ADC and data throughput
  + Talk with Rick Dekany about schedule and division of labor concerning the system level design