Meeting Notes April 12,2013

Attendees: Stephen Kaye, Pravin Chordia, Mahesh Burse

**Minutes**

* IUCAA posted an updated milestones document with dates on a quarterly timescale
* Status for the milestones will be updated by Tuesday
* Test results for bias loading were posted to the twiki. There appears to be some stray capacitance which will be investigated.
* Caltech posted the clock mapping for two CCDs which will go to one connector
* The Dump Drain voltage is higher than can be supplied by the current bias voltages.
* The Drain voltage for the all of the CCD amplifiers is at the upper limit of the present bias voltages.
* The nominal current for the CCD amplifiers is within the current available from the bias supply
* The number of clocks in the mapping is one higher than the number of supplied clocks. This must be resolved. Connecting the Dump Gate of the two separate CCDs is a potential solution.
* The current available from the clock drivers will allow acceptable rise times
* The new amplifier chosen for the pre-amp design was discussed. IUCAA will download the datasheet and look it over for any concerns.

**Action Items**

**IUCAA**

* + Will complete status column for the milestone document.
  + Will further investigate the capacitive loading in the bias load test
  + Will look over the ADA4897-2 op-amp and raise any concerns.

**Caltech**

* + Will look over IUCAA’s milestone document
  + Will investigate the nominal bias voltages
  + Will investigate reducing the clock count
  + Identify component matching requirements in design