IFPAC Milestones Ver 0.1

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| Sr No | Task Name | Start Date | Finish Date | Comments |
| 1 | Deliver Instructions on Waveform Generation |  |  | Instructions for CCD231-C6 or for 2k\*2k CCD? |
| 2 | Host Computer Interface Instructions Document  |  |  | Only for supported Commands |
| 3 | Test Data for Clock Board  |  |  | Basic Rise and fall time tests possible.  |
| 4 | Component Procurement and Assembly of Clock Driver Card  |  |  |  |
| 5 | ***Deliver Prototype Backplane Board, along with Cables to Caltech*** |  |  | Who delivers Computers and Power Source(s)? |
| 6 | Deliver Prototype Clock Board to Caltech |  |  | One month after test setup is ready (Power Supply)  |
| 7 | Test Data for Analog Board |  |  | ADC and Bias Voltage Tests? One month after test setup is ready  |
| 8 | Component Procurement and Assembly of Analog Card |  |  |  |
| 9 | Deliver prototype Analog Card (ADC and Bias Assembled) |  |  |  |
| 10 | ***Selection of Connectors, Cables and Interconnection Scheme, Between Cards i.e. Backplane Card, CCD Clocks, Biases and O/P connectors.***  |  |  | Need to understand in details interconnecting scheme for ZTF camera |
| 11 | Schematics for Preliminary Second Generation (2G) Clock Board |  |  |  |
| 12 | Schematics for Preliminary Second Generation (2G) Analog Card |  |  |  |
| 13 | ***Schematics for 2G for Backplane Card***  |  |  | ***See comments 7*** |
| 14 | Write up of preliminary 2G design Performance |  |  |  |
| 15 | IFPAC PDR |  |  |  |
| 16 | ***Post PDR Schematics for Backplane Board*** |  |  |  |
| 17 | Post PDR Schematics for Analog Board |  |  |  |
| 18 | Post PDR Schematics for Clock Board |  |  |  |
| 19 | Write up of 2G design Performance |  |  |  |
| 20 | ***Post PDR Connector, cables selection*** |  |  |  |
| 21 | ***PCB Designing of Preliminary Second Generation (2G) Backplane Card*** |  |  |  |
| 22 | ***Component procurement, PCB Fabrication and Assembly of Backplane Card*** |  |  |  |
| 23 | ***PCB Designing of Preliminary Second Generation (2G) Analog Card*** |  |  |  |
| 24 | ***Component procurement, PCB Fabrication and Assembly of Analog Card*** |  |  |  |
| 25 | ***PCB Designing of Preliminary Second Generation (2G) Clock Card***  |  |  |  |
| 26 | ***Component procurement, Fabrication and Assembly of Clock Card*** |  |  |  |
| 27 | ***Firmware development (VHDL)***  |  |  |  |
| 28 | ***Firmware Simulation*** |  |  |  |
| 29 | ***Host Software development*** |  |  |  |
| 30 | Test Data for 2G Clock Card |  |  |  |
| 31 | Test Data for 2G Analog Card |  |  |  |
| 32 | ***Test data of 2G Two Card System (Controller)***  |  |  |  |
| 33 | Deliver 2G two card Controller to Caltech |  |  |  |
| 34 | IFPAC FDR |  |  |  |
| 35 | ***Schematics for Final Backplane Card***  |  |  |  |
| 36 | Schematics for Final Analog Card  |  |  |  |
| 37 | Schematic for Final Clock Card  |  |  |  |
| 38 | Write up for Final Design Performance |  |  |  |
| 39 | ***PCB Designing of Final Backplane Card***  |  |  |  |
| 40 | ***Component procurement, PCB Fabrication and Assembly of Backplane Card*** |  |  |  |
| 41 | ***PCB Designing of Final Clock Card***  |  |  |  |
| 42 | ***Component procurement, PCB Fabrication and Assembly of Clock Card*** |  |  |  |
| 43 | ***PCB Designing of Final Analog Card***  |  |  |  |
| 44 | ***Component procurement, PCB Fabrication and Assembly of Clock Card*** |  |  |  |
| 45 | Test Data for Final Analog Card |  |  |  |
| 46 | Test Data for Final Analog Card |  |  |  |
| 47 | ***Test data of 2G Two Card System (Controller)*** |  |  |  |
| 48  | Begin Production of Controller Board Sets |  |  |  |