Meeting Notes March 22,2013

Attendees: Stephen Kaye, Roger Smith, Pravin Chordia, Mahesh Burse, A. N. Ramaprakash

**Minutes**

* IUCAA posted questions about the requirements document and these were discussed
* The number of bias lines and the number of bias lines sent to the CCD was clarified and will be updated in the requirements document
* The voltage range of the 16 higher voltage biases was clarified to be 0-27V
* The drive current for the biases was set to 50 mA and agreed upon by Caltech. The higher current drive in the requirements document came from the desire to power all output drains with one bias. This biasing will be changed to split up the bias lines for the output drains.
* There is a provision for filtering the bias lines on the backplane card. The filter uses ferrite beads and capacitors. A test will be done on a 1 kHz square wave to see if there are any resonances that need to be damped.
* The bias voltage stability requirement is too tight. It was agreed to reduce this to 50 mV sag at 50 mA load worst case. Lower impedance is better since it will reduce susceptibility to crosstalk. Our expectation is that the closed loop output impedance of the bias driver should be quite a bit less than this at low frequencies. Ie the closed loop output impedance should be the open loop output impedance (~20 ohm) divided by the loop gain. Thus <20 milliohm should be possible at low frequencies where trace and connector resistances (or the back plane filter impedance above) will begin to dominate, so we should set a new spec which is several times a measured value.
* A method for varying the bias load was suggested by Roger and will be drawn up and posted to the twiki. The idea is to create a transient load to see how much the bias output varies. By switching the load rapidly between two states, we also will see what the stability of bias driver is under load variations. In use these load variations can be CCD clock-to-bias crosstalk (eg SW to LG), switched loads such as the CCD reset, or current variations in the CCD output transistors as the signal varies. One way to generate a switched load (perhaps the best) is to connect a 100 ohm resistor from the bias output to an analog switch to ground. Another alternative to to connect the resistor to a 1KHz square wave generator with <10µs rise/fall times on the edges. Note: it is important to look for slow effects (<<1ms) which could be due to self heating and not just fast transients which are likely to be due to stability margin of the feedback loop for the bias driver.
* The summary of clock line capability was clarified. There are 30 clocks which swing +/- 10 V and 1 high voltage clock which swings 0 to 55V.
* For ZTF, the high voltage clock will not be used.
* A clarification was requested for the signal chain capabilities and tests. The document appears to only concern itself with the ADC performance and not the rest of the signal chain. This will be reviewed and updated, if needed.
* There is some confusion over the ADC voltage range and the output of the op-amps driving the ADC. A table of examples will be added to the requirements document to clarify the confusion. It is believed that this is only a disagreement on definitions.
* The dewar mounted preamp was discussed
* A question was raised on the digital signal controlling the black level clamp. Only one LVDS digital signal needs to be sent to the dewar. A LVDS receiver will fan out the logic to the preamps. This will be made explicit in the preamp documentation
* A short Caltech internal discussion was had on the need for the black level clamps. This will be followed up on at Caltech
* The bandwidth used to calculate the CCD amplifier noise may not be the correct bandwidth. This will be looked into further
* Caltech asked about timing waveform generation. The system is meant to be flexible without having to re-configure the FPGA. Caltech would like to have a prototype to familiarize ourselves with the IUCAA system
* Caltech will provide a schedule for testing, prototypes, and prototype deliverables

**Action Items**

**IUCAA**

* + Generate test data concerning the backplane bias filtering. A 100 kHz square wave will be tested for resonances.
  + Generate test data for the bias load regulation and stability using a variable load.
  + Provide power point presentation on questions and feedback concerning the preamp and video post-processor document
  + Review Caltech’s more refined milestone schedule and have comments.

**Caltech**

* + Will look at the mapping of bias signals to the CCD
  + Post a diagram describing the variable load test for the bias
  + Will review the requirements document. Make agreed upon changes/clarifications and post to twiki
  + Caltech will develop a more refined milestone and deliverables schedule. Document will be posted to the twiki on March 26th
  + Will provide a power point presentation for the video post processor design