Meeting Notes March 14,2013

Attendees: Stephen Kaye, Roger Smith, Pravin Chordia, Mahesh Burse

**Minutes**

* 1 clock card has been fully assembled and 2 clock cards are partially assembled
* 1 analog card has 2 channels assembled, but it needs a clock card in order to test
* The USB and Ethernet interfaces are being developed.
* Command line interface is presently being used to control the clock card
* All 64 DAC outputs can be set, but only 8 clocks can be generated now
* Only 8 clocks can be generated due to a power supply problem. There is insufficient current to run more clocks.
* Present power supply delivers 15V at 2A. The current draw at turn on causes the power supply to trip.
* Power supply is chassis mounted, not a bench top lab supply.
* Suggestion to ramp up power supply voltage not possible with present supply since it is not variable.
* For the 8 working clocks, 300 pF capacitor loads are used to simulate the CCD
* Have measured 30 nsec rise time for 1.2 MHz clock with 300 pF load
* Software exists to load and generate clocks for an e2v 42-40, which is in hand
* Analog card has 2 bias channels populated: a +/-15V bias and a 0/+30V bias
* Clock card can read ADC data from analog card. IUCAA is getting ready to test the noise.
* Testing/requirements document has been received by IUCAA. Only had time for a quick glance. Will provide notes, questions, and feedback before next meeting.
* Schedule from IUCAA needs consultation with Ram. Division of effort with other projects needs to be discussed
* Caltech asked about timing waveform generation. The system is meant to be flexible without having to re-configure the FPGA. Caltech would like to have a prototype to familiarize ourselves with the IUCAA system
* Caltech will provide a schedule for testing, prototypes, and prototype deliverables

**Action Items**

**IUCAA**

* + IUCAA will provide a schedule document. The milestones will also include dates for reviews of designs and reviews of performance tests.
	+ IUCAA will provide comments and questions concerning the testing and requirements document
	+ Will provide a power point presentation for the two items above to be posted to the twiki a day before the meeting

 **Caltech**

* + Caltech will finish and post the document describing performance of pre-amp and ideas for a fully digital CDS. Document will be posted to twiki.
	+ Caltech will develop a more refined milestone and deliverables schedule. Document will be posted to the twiki
	+ Will provide a power point presentation for the two items above to be posted to the twiki a day before the meeting