**Requirements and Testing Plan for IUCCA Focal Plane Array Controller**

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# Introduction

Focal plane CCDs at Palomar are ubiquitous and need support electronics for biasing and image acquisition. It is advantageous to have the support electronics close to the CCD, and so the packaging of the controller electronics is an important aspect of the system. The performance of the astronomical instrument is directly related to the performance of the controller electronics. In this note, we describe the electrical specifications for the controller and the tests necessary to confirm the electrical performance.

# Electrical

## Biases

The bias lines on the analog card are used for powering the CCD output amplifier and associated circuitry. These bias lines need to be stable, low-noise, and free from transients. This section will discuss the capabilities of the analog bias lines along with the noise suppression scheme and circuitry.

### Summary of Capabilities

A quick summary of the bias requirements is shown in Table 1. Note this requirement is for controlling a single CCD, and the controller is required to be able to control up to 2 CCDs. A total of 24 biases must be supplied for each CCD with different voltage ranges. These voltage ranges will accommodate the powering of CCD output circuitry and static gates and drains. The higher voltage range will be used to power Reset Drains, Output Drains, Dump Drains, and other biases. The lower voltage range will be used to power Output Gates.

|  |  |  |  |
| --- | --- | --- | --- |
| Number of Biases | Voltage Range | Voltage Resolution | Current Capability |
| 8 | -12V to +12V | 8 bit | 250 mA |
| 16 | 0V to +30V | 8 bit | 250 mA |

Table 1: Analog Bias Voltage Capabilities

For both sets of voltage ranges, the voltage resolution is 8 bits. This implies a 93.8 mV step for the lower voltage range and a 117.2 mV step for the higher voltage range.

### Testing Procedures

Each analog bias must be tested at each bias level and with an appropriate load. These tests can be performed with either a digitizing oscilloscope or a data acquisition card which can accept the full range of analog bias voltages and can measure down to 0.5 mV. The load should be a parallel combination of a resistor and a capacitor. The resistor value should test the current capacity of the bias line while the capacitor should be an approximation of the capacitance seen on a typical gate. Use 200 pF for the load capacitance.

**Bias Voltage Noise**

For each voltage level of each bias, collect 10,000 data points at each voltage level at a conversion speed of 1 MHz (2.65 seconds). For each voltage level, plot a histogram of the data and report the width of the resultant Gaussian (rms voltage noise). The maximum width of any of the histograms in the group must be less than 1 mV.

**Bias DAC Linearity**

Use the center value of each Gaussian from the bias voltage noise data and graph the center value versus the DAC input code to test linearity of the DAC. Use a best fit to a line to determine the gain and offset. The differential linearity is calculated from the equation1:

$$DNL\left(i\right)= \frac{\left(S\left(i+1\right)-S\left(i\right)- V\_{lsb}\right)}{V\_{lsb}}$$

Where S(i) is the output voltage of the ith code, and Vlsb is the designed LSB voltage (93.8 mV/LSB for the lower voltage range and 117.2 mV/LSB for the higher voltage range). Report the maximum DNL for each bias voltage. Maximum DNL must be less than 1 LSB.

The integral non-linearity is calculated from the equation1:

$$INL\left(i\right)= \frac{\left(S\left(i\right)- \left(m\_{best-fit}\* i\_{0}+ b\_{best-fit}\right)\right)}{V\_{lsb}}$$

Where S(i) is again the output voltage of the ith code, mbest-fit and bbest-fit are the gain and offset of the best fit line, and i0 is the input digital code for S(0). Maximum INL must be less than 1 LSB.

**Bias Voltage Range**

Test the bias voltage at its maximum and minimum output voltage. Input the DAC code for the maximum voltage output and measure the output voltage. Repeat this test for each low voltage and high voltage bias channel. The minimum output voltage should be tested as well. Input the DAC code for the minimum voltage output and measure the output voltage. For the low voltage bias channels, the maximum output voltage must be equal to or greater than +12 V, and the minimum output voltage must be less than or equal to -12 V. For the high voltage bias channels, the maximum output voltage must be equal to or greater than +30 V, and the minimum output voltage must be less than or equal to 0 V.

**Bias Voltage Drive Current**

Measure the maximum bias voltage before and after a load of 250 mA is placed on the output. A large deviation suggests insufficient drive current. Collect 10,000 data points of the maximum bias voltage at a conversion speed of 1 MHz with a load of 250 mA. Compare the center value of the resultant Gaussian with the center value of the unloaded maximum bias voltage. Report the difference between unloaded and loaded bias voltages. The maximum deviation should be less than the RMS bias voltage noise.

**Capacitive Load Test**

The bias lines may drive a capacitive load such as the last gate. A quick test for stable operation driving a capacitive load is needed. Connect each bias line to a capacitive load of 200 pF and set the output to the highest bias voltage for the channel. Record if oscillation occurs. Repeat the test with setting the bias voltage to the minimum voltage for each channel. Record if oscillation occurs.

## Clock Lines

The digital card provides all of the clock signals to the detector system. In addition to providing the clock signals, the digital card programs the DACs for the clock voltage rails and the analog bias voltages. This is accomplished with the Virtex FPGA from Xilinx. The digital card must also handle the digitized image data. This section will discuss the clock drivers and the testing that must be done.

### Summary of Capabilities

The digital board provides 30 clock signals with a programmable voltage range from -10 V to +10 V. The current drive capability is 300 mA for each clock driver. One additional high voltage clock is provided which can be programmed for operation up to 60 V for electron multiplied CCDs and deep depletion CCDs. DACs are used to provide the programmable voltage rails. Testing must be done on the clock voltage rails, the switching speed, the capacitive load driving capability, and the clock voltage noise.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Number of Clocks | Maximum High Voltage Rail | Minimum Low Voltage Rail | Maximum Capacitive Load | Maximum Switching Speed |
| 29 | +10V | -10V | 300 pF | 1 MHz |
| 1 | +60V | -10V | 300 pF | 1 MHz |

Table 2: Clock Capabilities

### Testing Procedures

Each rail of the clock signal must be fully tested at each voltage level. These tests can be performed with either a digitizing oscilloscope or a data acquisition card which can accept the full range of the clock rail voltages and can measure down to 0.5 mV.

**Clock Rail Voltage Noise**

This tests the noise of the DAC that is providing the voltage for each clock rail. The clock rail DAC has 8 bit resolution and must be tested through the entire range of voltages. For each voltage level of each clock rail, collect 10,000 data points at a conversion speed of 1 MHz (2.65 seconds). For each voltage level, plot a histogram of the data and report the width of the resultant Gaussian (rms voltage noise). The maximum width of the group of histograms must be less than TBD mV. This test should be performed for both the high clock rail and the low clock rail.

**Clock Rail DAC Linearity**

This section is to test the linearity of the DAC providing the voltage for the clock rails. It is similar to the test for the bias voltages. Use the center value of each Gaussian from the clock rail voltage noise data and graph the center value versus the DAC input code to test linearity of the DAC. Use a best fit to a line to determine the gain and offset. The differential linearity is calculated from the equation1:

$$DNL\left(i\right)= \frac{\left(S\left(i+1\right)-S\left(i\right)- V\_{lsb}\right)}{V\_{lsb}}$$

Where S(i) is the output voltage of the ith code, and Vlsb is the designed LSB voltage (???). Report the maximum DNL for each bias voltage. Maximum DNL must be less than 1 LSB.

The integral non-linearity is calculated from the equation1:

$$INL\left(i\right)= \frac{\left(S\left(i\right)- \left(m\_{best-fit}\* i\_{0}+ b\_{best-fit}\right)\right)}{V\_{lsb}}$$

Where S(i) is again the output voltage of the ith code, mbest-fit and bbest-fit are the gain and offset of the best fit line, and i0 is the input digital code for S(0). Maximum INL must be less than 1 LSB.

**Clock Rail Voltage Range**

This is to test the high and low clock rail voltages. For each of the high clock rails, input the DAC code for the maximum voltage output and measure the output voltage. Repeat this test for each high rail for all clock channels. The minimum output voltage for the low clock rail should be tested as well. For each of the low clock rails, input the DAC code for the minimum voltage output and measure the output voltage. For the low voltage clock channels, the maximum output voltage for the high rail must be equal to or greater than +10 V, and the minimum output voltage for the low rail must be less than or equal to -10 V. For the high voltage clock channel, the maximum output voltage for the high rail must be equal to or greater than +60 V, and the minimum output voltage for the low rail must be less than or equal to -10 V.

**Clock Switching Speed and Settling Time**

This is to test the switching speed and stability of the clocks when driving capacitive loads. This test must be performed with a worst-case capacitive load since all clocks are presumed to be equal in their driving capabilities. The CCD controller must be able to read out a CCD at a 1 Mpixel/second rate and so all the clocks must be tested at the maximum clock speed of 1 MHz. The largest capacitive load for a clock is 300 pF for the phase 1 serial clock.

Use a 300 pF capacitive load on each clock and exercise it at 1 MHz. The clock rails should be set to the maximum high rail and minimum low rail (i.e. +10 V to -10 V for the regular clocks and +60 V to -10 V for the high voltage clock). Make sure no oscillation is occurring on the clock channel. Measure the rise time and fall time of the clock signal. The maximum rise and fall time should be no more than 40 nsec.

Measure the voltage on the high clock rail and the low clock rail. Check these against the maximum high and low clock rail voltages measured in the previous section’s test.

Measure the settling time of the clock signal. The settling time is the time it takes the signal to stay within 0.01 % of the rail voltage. For the typical clock, the settling time is the time it takes for the clock to stay within 1 mV of the 10 V high rail. Similarly, the settling time for the low rail is made in the same way.

## Signal Chain

The signal chain is the heart of the analog board. The amplifier chain conditions the CCD video signal and converts the analog signal to digital information to be saved in an image file. The signal conditioning is paramount to achieving low noise performance of the detector system. The signal chain amplifies the video to a useable level and performs correlated double sampling (CDS) to create a final signal voltage which is then converted to a digital number. The gain of the signal chain is selectable along with the time constant for the CDS integration.

### Summary of Capabilities

The analog board provides 8 channels of video processing. Each video input is capacitively coupled to the video processing signal chain. The differential voltage range for the video signal is from -4.096 V to + 4.096V. Correlated double sampling (CDS) is performed on the analog signal to account for any residual charge on the reset signal. The output of each video processing channel is digital image data with a resolution of 16 bits. The image conversion speed is 1 Mpixel/second.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Number of Video Channels | Maximum Differential Input | Minimum Differential Input | Maximum Pixel Conversion | Conversion Resolution |
| 8 | +4.096 V | -4.096 V | 1 Mpixel/second | 16 bits |

Table 3: Clock Capabilities

### Signal Chain Tests

Histogram testing is used to determine offset errors and INL and DNL errors. For this test, a triangular waveform is injected into the signal chain and the ADC converts the data at 1MHz. The input waveform and conversions are asynchronous. The input waveform must have an amplitude equal to the input range of the ADC. This method will eventually produce every code of the ADC. A minimum of about 70 Msamples must be collected to calculate the DNL and INL.

This testing document proposes that for initial testing, a waveform generator creates the input signal for this test. For the long term, devising a method for performing this test in-situ is desired. Please refer to Reference 2 and Reference 3 for further reading on this method.

**ADC Offset Error**

Determine the offset error of the ADC. For the ADC7625, this can be found by testing the zero error. Zero all programmable offsets along the signal chain. Apply a signal which produces 0V differential at the ADC. Take 1000 samples at 1MHz. The average of the samples is the offset error. Record this value. Adjust the programmable offset so that the average code from the ADC is 0V. Record the programmed DAC value. Repeat for each analog channel. Maximum allowable offset error is ±1.5 LSB.

**INL/DNL and Missing Codes**

Apply 10 Hz triangle wave to the input of the signal chain and use single sample integration. The amplitude of the triangle wave should cover the entire ADC range. Each ADC value is equally likely to be acquired. Acquire enough data at 1MHz sampling so that each ADC code occurs 1000 times on average. A histogram of the entire data set should be flat. Report any missing codes from the data set or anomalies in the histogram. Repeat for each analog channel. No missing codes are allowed.

This test set up also can measure the integral and differential non-linearity of the ADC. Using the histogram, the differential non-linearity can be calculated from the following equation2:

$$DN\left(i\right)= \frac{{H\left(i\right)}/{N\_{t}}}{P\left(i\right)}-1$$

Where H(i) is the number of counts in the ith bin and Nt is the total number of samples, and P(i) is the ideal bin width.

Please refer to Reference 3 for a calculation if the integral non-linearity.

**ADC/Signal Chain Noise**

Apply a known low-noise voltage to the input of the signal chain. This voltage must have a voltage noise of less than 60 µV and must be adjustable over the range of the ADC reference voltage. Acquire 10,000 samples at 1 MHz for the voltage at each ADC code center. Make a histogram for each data set. Report the width of the histogram at each voltage setting. Repeat for each analog channel. The maximum RMS noise for all of the ADC conversion should be less than 1 LSB.

# Appendix

## Bias Voltage Test Sheets

This section contains tables to be filled out while testing the bias lines.

Bias Voltage Noise

Low Voltage Biases

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum RMS Voltage Noise | Tested Value | Pass |
| 1 | 1 mV |  |  |
| 2 | 1 mV |  |  |
| 3 | 1 mV |  |  |
| 4 | 1 mV |  |  |
| 5 | 1 mV |  |  |
| 6 | 1 mV |  |  |
| 7 | 1 mV |  |  |
| 8 | 1 mV |  |  |

High Voltage Biases

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum RMS Voltage Noise | Tested Value | Pass |
| 1 | 1 mV |  |  |
| 2 | 1 mV |  |  |
| 3 | 1 mV |  |  |
| 4 | 1 mV |  |  |
| 5 | 1 mV |  |  |
| 6 | 1 mV |  |  |
| 7 | 1 mV |  |  |
| 8 | 1 mV |  |  |
| 9 | 1 mV |  |  |
| 10 | 1 mV |  |  |
| 11 | 1 mV |  |  |
| 12 | 1 mV |  |  |
| 13 | 1 mV |  |  |
| 14 | 1 mV |  |  |
| 15 | 1 mV |  |  |
| 16 | 1 mV |  |  |

Bias DAC Linearity

Low Voltage Biases Differential Non-Linearity

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum DNL | Tested Value | Pass |
| 1 | 1 LSB |  |  |
| 2 | 1 LSB |  |  |
| 3 | 1 LSB |  |  |
| 4 | 1 LSB |  |  |
| 5 | 1 LSB |  |  |
| 6 | 1 LSB |  |  |
| 7 | 1 LSB |  |  |
| 8 | 1 LSB |  |  |

High Voltage Biases Differential Non-Linearity

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum DNL | Tested Value | Pass |
| 1 | 1 LSB |  |  |
| 2 | 1 LSB |  |  |
| 3 | 1 LSB |  |  |
| 4 | 1 LSB |  |  |
| 5 | 1 LSB |  |  |
| 6 | 1 LSB |  |  |
| 7 | 1 LSB |  |  |
| 8 | 1 LSB |  |  |
| 9 | 1 LSB |  |  |
| 10 | 1 LSB |  |  |
| 11 | 1 LSB |  |  |
| 12 | 1 LSB |  |  |
| 13 | 1 LSB |  |  |
| 14 | 1 LSB |  |  |
| 15 | 1 LSB |  |  |
| 16 | 1 LSB |  |  |

Low Voltage Biases Integral Non-Linearity

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum INL | Tested Value | Pass |
| 1 | 1 LSB |  |  |
| 2 | 1 LSB |  |  |
| 3 | 1 LSB |  |  |
| 4 | 1 LSB |  |  |
| 5 | 1 LSB |  |  |
| 6 | 1 LSB |  |  |
| 7 | 1 LSB |  |  |
| 8 | 1 LSB |  |  |

High Voltage Biases Integral Non-Linearity

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum INL | Tested Value | Pass |
| 1 | 1 LSB |  |  |
| 2 | 1 LSB |  |  |
| 3 | 1 LSB |  |  |
| 4 | 1 LSB |  |  |
| 5 | 1 LSB |  |  |
| 6 | 1 LSB |  |  |
| 7 | 1 LSB |  |  |
| 8 | 1 LSB |  |  |
| 9 | 1 LSB |  |  |
| 10 | 1 LSB |  |  |
| 11 | 1 LSB |  |  |
| 12 | 1 LSB |  |  |
| 13 | 1 LSB |  |  |
| 14 | 1 LSB |  |  |
| 15 | 1 LSB |  |  |
| 16 | 1 LSB |  |  |

Voltage swing capabilities

Low Voltage Biases

Positive Rail Test

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Minimum Positive Full Scale Voltage | Tested Value | Pass |
| 1 | +12 V |  |  |
| 2 | +12 V |  |  |
| 3 | +12 V |  |  |
| 4 | +12 V |  |  |
| 5 | +12 V |  |  |
| 6 | +12 V |  |  |
| 7 | +12 V |  |  |
| 8 | +12 V |  |  |

Negative Rail Test

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum Negative Full Scale Voltage | Tested Value | Pass |
| 1 | -12 V |  |  |
| 2 | -12 V |  |  |
| 3 | -12 V |  |  |
| 4 | -12 V |  |  |
| 5 | -12 V |  |  |
| 6 | -12 V |  |  |
| 7 | -12 V |  |  |
| 8 | -12 V |  |  |

High Voltage Biases

Positive Rail Test

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Minimum Positive Full Scale Voltage | Tested Value | Pass |
| 1 | +30 V |  |  |
| 2 | +30 V |  |  |
| 3 | +30 V |  |  |
| 4 | +30 V |  |  |
| 5 | +30 V |  |  |
| 6 | +30 V |  |  |
| 7 | +30 V |  |  |
| 8 | +30 V |  |  |
| 9 | +30 V |  |  |
| 10 | +30 V |  |  |
| 11 | +30 V |  |  |
| 12 | +30 V |  |  |
| 13 | +30 V |  |  |
| 14 | +30 V |  |  |
| 15 | +30 V |  |  |
| 16 | +30 V |  |  |

Negative (Low) Rail Test

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Minimum Positive Full Scale Voltage | Tested Value | Pass |
| 1 | 0 V |  |  |
| 2 | 0 V |  |  |
| 3 | 0 V |  |  |
| 4 | 0 V |  |  |
| 5 | 0 V |  |  |
| 6 | 0 V |  |  |
| 7 | 0 V |  |  |
| 8 | 0 V |  |  |
| 9 | 0 V |  |  |
| 10 | 0 V |  |  |
| 11 | 0 V |  |  |
| 12 | 0 V |  |  |
| 13 | 0 V |  |  |
| 14 | 0 V |  |  |
| 15 | 0 V |  |  |
| 16 | 0 V |  |  |

Voltage Drive Capabilities

Low Voltage Biases

Positive Rail Test

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum Deviation for Bias Voltage Delivering 50 mA | Tested Value | Pass |
| 1 | RMS Voltage Noise |  |  |
| 2 | RMS Voltage Noise |  |  |
| 3 | RMS Voltage Noise |  |  |
| 4 | RMS Voltage Noise |  |  |
| 5 | RMS Voltage Noise |  |  |
| 6 | RMS Voltage Noise |  |  |
| 7 | RMS Voltage Noise |  |  |
| 8 | RMS Voltage Noise |  |  |

Negative Rail Test

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum Deviation for Bias Voltage Delivering 50 mA | Tested Value | Pass |
| 1 | RMS Voltage Noise |  |  |
| 2 | RMS Voltage Noise |  |  |
| 3 | RMS Voltage Noise |  |  |
| 4 | RMS Voltage Noise |  |  |
| 5 | RMS Voltage Noise |  |  |
| 6 | RMS Voltage Noise |  |  |
| 7 | RMS Voltage Noise |  |  |
| 8 | RMS Voltage Noise |  |  |

High Voltage Biases

Positive Rail Test

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum Deviation for Bias Voltage Delivering 5 mA | Tested Value | Pass |
| 1 | RMS Voltage Noise |  |  |
| 2 | RMS Voltage Noise |  |  |
| 3 | RMS Voltage Noise |  |  |
| 4 | RMS Voltage Noise |  |  |
| 5 | RMS Voltage Noise |  |  |
| 6 | RMS Voltage Noise |  |  |
| 7 | RMS Voltage Noise |  |  |
| 8 | RMS Voltage Noise |  |  |
| 9 | RMS Voltage Noise |  |  |
| 10 | RMS Voltage Noise |  |  |
| 11 | RMS Voltage Noise |  |  |
| 12 | RMS Voltage Noise |  |  |
| 13 | RMS Voltage Noise |  |  |
| 14 | RMS Voltage Noise |  |  |
| 15 | RMS Voltage Noise |  |  |
| 16 | RMS Voltage Noise |  |  |

Negative Rail Test

|  |  |  |  |
| --- | --- | --- | --- |
| Bias | Maximum Deviation for Bias Voltage Delivering 5 mA | Tested Value | Pass |
| 1 | RMS Voltage Noise |  |  |
| 2 | RMS Voltage Noise |  |  |
| 3 | RMS Voltage Noise |  |  |
| 4 | RMS Voltage Noise |  |  |
| 5 | RMS Voltage Noise |  |  |
| 6 | RMS Voltage Noise |  |  |
| 7 | RMS Voltage Noise |  |  |
| 8 | RMS Voltage Noise |  |  |
| 9 | RMS Voltage Noise |  |  |
| 10 | RMS Voltage Noise |  |  |
| 11 | RMS Voltage Noise |  |  |
| 12 | RMS Voltage Noise |  |  |
| 13 | RMS Voltage Noise |  |  |
| 14 | RMS Voltage Noise |  |  |
| 15 | RMS Voltage Noise |  |  |
| 16 | RMS Voltage Noise |  |  |

## Clock Test Sheets

Clock Voltage Noise

High Rail Clock Biases

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Maximum RMS Voltage Noise | Tested Value | Pass |
| 1 | 1 mV |  |  |
| 2 | 1 mV |  |  |
| 3 | 1 mV |  |  |
| 4 | 1 mV |  |  |
| 5 | 1 mV |  |  |
| 6 | 1 mV |  |  |
| 7 | 1 mV |  |  |
| 8 | 1 mV |  |  |
| 9 | 1 mV |  |  |
| 10 | 1 mV |  |  |
| 11 | 1 mV |  |  |
| 12 | 1 mV |  |  |
| 13 | 1 mV |  |  |
| 14 | 1 mV |  |  |
| 15 | 1 mV |  |  |
| 16 | 1 mV |  |  |
| 17 | 1 mV |  |  |
| 18 | 1 mV |  |  |
| 19 | 1 mV |  |  |
| 20 | 1 mV |  |  |
| 21 | 1 mV |  |  |
| 22 | 1 mV |  |  |
| 23 | 1 mV |  |  |
| 24 | 1 mV |  |  |
| 25 | 1 mV |  |  |
| 26 | 1 mV |  |  |
| 27 | 1 mV |  |  |
| 28 | 1 mV |  |  |
| 29 | 1 mV |  |  |
| 30 | 1 mV |  |  |

Low Rail Clock Biases

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Maximum RMS Voltage Noise | Tested Value | Pass |
| 1 | 1 mV |  |  |
| 2 | 1 mV |  |  |
| 3 | 1 mV |  |  |
| 4 | 1 mV |  |  |
| 5 | 1 mV |  |  |
| 6 | 1 mV |  |  |
| 7 | 1 mV |  |  |
| 8 | 1 mV |  |  |
| 9 | 1 mV |  |  |
| 10 | 1 mV |  |  |
| 11 | 1 mV |  |  |
| 12 | 1 mV |  |  |
| 13 | 1 mV |  |  |
| 14 | 1 mV |  |  |
| 15 | 1 mV |  |  |
| 16 | 1 mV |  |  |
| 17 | 1 mV |  |  |
| 18 | 1 mV |  |  |
| 19 | 1 mV |  |  |
| 20 | 1 mV |  |  |
| 21 | 1 mV |  |  |
| 22 | 1 mV |  |  |
| 23 | 1 mV |  |  |
| 24 | 1 mV |  |  |
| 25 | 1 mV |  |  |
| 26 | 1 mV |  |  |
| 27 | 1 mV |  |  |
| 28 | 1 mV |  |  |
| 29 | 1 mV |  |  |
| 30 | 1 mV |  |  |

Clock Rail DAC Linearity

High Rail Clock Differential Non-Linearity

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Maximum DNL | Tested Value | Pass |
| 1 | 1 LSB |  |  |
| 2 | 1 LSB |  |  |
| 3 | 1 LSB |  |  |
| 4 | 1 LSB |  |  |
| 5 | 1 LSB |  |  |
| 6 | 1 LSB |  |  |
| 7 | 1 LSB |  |  |
| 8 | 1 LSB |  |  |
| 9 | 1 LSB |  |  |
| 10 | 1 LSB |  |  |
| 11 | 1 LSB |  |  |
| 12 | 1 LSB |  |  |
| 13 | 1 LSB |  |  |
| 14 | 1 LSB |  |  |
| 15 | 1 LSB |  |  |
| 16 | 1 LSB |  |  |
| 17 | 1 LSB |  |  |
| 18 | 1 LSB |  |  |
| 19 | 1 LSB |  |  |
| 20 | 1 LSB |  |  |
| 21 | 1 LSB |  |  |
| 22 | 1 LSB |  |  |
| 23 | 1 LSB |  |  |
| 24 | 1 LSB |  |  |
| 25 | 1 LSB |  |  |
| 26 | 1 LSB |  |  |
| 27 | 1 LSB |  |  |
| 28 | 1 LSB |  |  |
| 29 | 1 LSB |  |  |
| 30 | 1 LSB |  |  |

Low Rail Clock Differential Non-Linearity

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Maximum DNL | Tested Value | Pass |
| 1 | 1 LSB |  |  |
| 2 | 1 LSB |  |  |
| 3 | 1 LSB |  |  |
| 4 | 1 LSB |  |  |
| 5 | 1 LSB |  |  |
| 6 | 1 LSB |  |  |
| 7 | 1 LSB |  |  |
| 8 | 1 LSB |  |  |
| 9 | 1 LSB |  |  |
| 10 | 1 LSB |  |  |
| 11 | 1 LSB |  |  |
| 12 | 1 LSB |  |  |
| 13 | 1 LSB |  |  |
| 14 | 1 LSB |  |  |
| 15 | 1 LSB |  |  |
| 16 | 1 LSB |  |  |
| 17 | 1 LSB |  |  |
| 18 | 1 LSB |  |  |
| 19 | 1 LSB |  |  |
| 20 | 1 LSB |  |  |
| 21 | 1 LSB |  |  |
| 22 | 1 LSB |  |  |
| 23 | 1 LSB |  |  |
| 24 | 1 LSB |  |  |
| 25 | 1 LSB |  |  |
| 26 | 1 LSB |  |  |
| 27 | 1 LSB |  |  |
| 28 | 1 LSB |  |  |
| 29 | 1 LSB |  |  |
| 30 | 1 LSB |  |  |

High Rail Clock Integral Non-Linearity

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Maximum INL | Tested Value | Pass |
| 1 | 1 LSB |  |  |
| 2 | 1 LSB |  |  |
| 3 | 1 LSB |  |  |
| 4 | 1 LSB |  |  |
| 5 | 1 LSB |  |  |
| 6 | 1 LSB |  |  |
| 7 | 1 LSB |  |  |
| 8 | 1 LSB |  |  |
| 9 | 1 LSB |  |  |
| 10 | 1 LSB |  |  |
| 11 | 1 LSB |  |  |
| 12 | 1 LSB |  |  |
| 13 | 1 LSB |  |  |
| 14 | 1 LSB |  |  |
| 15 | 1 LSB |  |  |
| 16 | 1 LSB |  |  |
| 17 | 1 LSB |  |  |
| 18 | 1 LSB |  |  |
| 19 | 1 LSB |  |  |
| 20 | 1 LSB |  |  |
| 21 | 1 LSB |  |  |
| 22 | 1 LSB |  |  |
| 23 | 1 LSB |  |  |
| 24 | 1 LSB |  |  |
| 25 | 1 LSB |  |  |
| 26 | 1 LSB |  |  |
| 27 | 1 LSB |  |  |
| 28 | 1 LSB |  |  |
| 29 | 1 LSB |  |  |
| 30 | 1 LSB |  |  |

Low Rail Clock Integral Non-Linearity

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Maximum INL | Tested Value | Pass |
| 1 | 1 LSB |  |  |
| 2 | 1 LSB |  |  |
| 3 | 1 LSB |  |  |
| 4 | 1 LSB |  |  |
| 5 | 1 LSB |  |  |
| 6 | 1 LSB |  |  |
| 7 | 1 LSB |  |  |
| 8 | 1 LSB |  |  |
| 9 | 1 LSB |  |  |
| 10 | 1 LSB |  |  |
| 11 | 1 LSB |  |  |
| 12 | 1 LSB |  |  |
| 13 | 1 LSB |  |  |
| 14 | 1 LSB |  |  |
| 15 | 1 LSB |  |  |
| 16 | 1 LSB |  |  |
| 17 | 1 LSB |  |  |
| 18 | 1 LSB |  |  |
| 19 | 1 LSB |  |  |
| 20 | 1 LSB |  |  |
| 21 | 1 LSB |  |  |
| 22 | 1 LSB |  |  |
| 23 | 1 LSB |  |  |
| 24 | 1 LSB |  |  |
| 25 | 1 LSB |  |  |
| 26 | 1 LSB |  |  |
| 27 | 1 LSB |  |  |
| 28 | 1 LSB |  |  |
| 29 | 1 LSB |  |  |
| 30 | 1 LSB |  |  |

Rail Voltage swing capabilities

Positive Rail Test

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Minimum Positive Full Scale Voltage | Tested Value | Pass |
| 1 | 10 V |  |  |
| 2 | 10 V |  |  |
| 3 | 10 V |  |  |
| 4 | 10 V |  |  |
| 5 | 10 V |  |  |
| 6 | 10 V |  |  |
| 7 | 10 V |  |  |
| 8 | 10 V |  |  |
| 9 | 10 V |  |  |
| 10 | 10 V |  |  |
| 11 | 10 V |  |  |
| 12 | 10 V |  |  |
| 13 | 10 V |  |  |
| 14 | 10 V |  |  |
| 15 | 10 V |  |  |
| 16 | 10 V |  |  |
| 17 | 10 V |  |  |
| 18 | 10 V |  |  |
| 19 | 10 V |  |  |
| 20 | 10 V |  |  |
| 21 | 10 V |  |  |
| 22 | 10 V |  |  |
| 23 | 10 V |  |  |
| 24 | 10 V |  |  |
| 25 | 10 V |  |  |
| 26 | 10 V |  |  |
| 27 | 10 V |  |  |
| 28 | 10 V |  |  |
| 29 | 10 V |  |  |
| 30 | 60 V |  |  |

Negative Rail Test

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Maximum Negative Full Scale Voltage | Tested Value | Pass |
| 1 | -10 V |  |  |
| 2 | -10 V |  |  |
| 3 | -10 V |  |  |
| 4 | -10 V |  |  |
| 5 | -10 V |  |  |
| 6 | -10 V |  |  |
| 7 | -10 V |  |  |
| 8 | -10 V |  |  |
| 9 | -10 V |  |  |
| 10 | -10 V |  |  |
| 11 | -10 V |  |  |
| 12 | -10 V |  |  |
| 13 | -10 V |  |  |
| 14 | -10 V |  |  |
| 15 | -10 V |  |  |
| 16 | -10 V |  |  |
| 17 | -10 V |  |  |
| 18 | -10 V |  |  |
| 19 | -10 V |  |  |
| 20 | -10 V |  |  |
| 21 | -10 V |  |  |
| 22 | -10 V |  |  |
| 23 | -10 V |  |  |
| 24 | -10 V |  |  |
| 25 | -10 V |  |  |
| 26 | -10 V |  |  |
| 27 | -10 V |  |  |
| 28 | -10 V |  |  |
| 29 | -10 V |  |  |
| 30 | -10 V |  |  |

Clock rise and fall times/Stability

Clock Oscillation

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Oscillation Allowable | Tested Value | Pass |
| 1 | No |  |  |
| 2 | No |  |  |
| 3 | No |  |  |
| 4 | No |  |  |
| 5 | No |  |  |
| 6 | No |  |  |
| 7 | No |  |  |
| 8 | No |  |  |
| 9 | No |  |  |
| 10 | No |  |  |
| 11 | No |  |  |
| 12 | No |  |  |
| 13 | No |  |  |
| 14 | No |  |  |
| 15 | No |  |  |
| 16 | No |  |  |
| 17 | No |  |  |
| 18 | No |  |  |
| 19 | No |  |  |
| 20 | No |  |  |
| 21 | No |  |  |
| 22 | No |  |  |
| 23 | No |  |  |
| 24 | No |  |  |
| 25 | No |  |  |
| 26 | No |  |  |
| 27 | No |  |  |
| 28 | No |  |  |
| 29 | No |  |  |
| 30 | No |  |  |

Clock Rise Time

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Maximum Rise Time | Tested Value | Pass |
| 1 | 40 nsec |  |  |
| 2 | 40 nsec |  |  |
| 3 | 40 nsec |  |  |
| 4 | 40 nsec |  |  |
| 5 | 40 nsec |  |  |
| 6 | 40 nsec |  |  |
| 7 | 40 nsec |  |  |
| 8 | 40 nsec |  |  |
| 9 | 40 nsec |  |  |
| 10 | 40 nsec |  |  |
| 11 | 40 nsec |  |  |
| 12 | 40 nsec |  |  |
| 13 | 40 nsec |  |  |
| 14 | 40 nsec |  |  |
| 15 | 40 nsec |  |  |
| 16 | 40 nsec |  |  |
| 17 | 40 nsec |  |  |
| 18 | 40 nsec |  |  |
| 19 | 40 nsec |  |  |
| 20 | 40 nsec |  |  |
| 21 | 40 nsec |  |  |
| 22 | 40 nsec |  |  |
| 23 | 40 nsec |  |  |
| 24 | 40 nsec |  |  |
| 25 | 40 nsec |  |  |
| 26 | 40 nsec |  |  |
| 27 | 40 nsec |  |  |
| 28 | 40 nsec |  |  |
| 29 | 40 nsec |  |  |
| 30 | 40 nsec |  |  |

Clock Fall Time

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Maximum Fall Time | Tested Value | Pass |
| 1 | 40 nsec |  |  |
| 2 | 40 nsec |  |  |
| 3 | 40 nsec |  |  |
| 4 | 40 nsec |  |  |
| 5 | 40 nsec |  |  |
| 6 | 40 nsec |  |  |
| 7 | 40 nsec |  |  |
| 8 | 40 nsec |  |  |
| 9 | 40 nsec |  |  |
| 10 | 40 nsec |  |  |
| 11 | 40 nsec |  |  |
| 12 | 40 nsec |  |  |
| 13 | 40 nsec |  |  |
| 14 | 40 nsec |  |  |
| 15 | 40 nsec |  |  |
| 16 | 40 nsec |  |  |
| 17 | 40 nsec |  |  |
| 18 | 40 nsec |  |  |
| 19 | 40 nsec |  |  |
| 20 | 40 nsec |  |  |
| 21 | 40 nsec |  |  |
| 22 | 40 nsec |  |  |
| 23 | 40 nsec |  |  |
| 24 | 40 nsec |  |  |
| 25 | 40 nsec |  |  |
| 26 | 40 nsec |  |  |
| 27 | 40 nsec |  |  |
| 28 | 40 nsec |  |  |
| 29 | 40 nsec |  |  |
| 30 | 40 nsec |  |  |

Clock Settling Time

|  |  |  |  |
| --- | --- | --- | --- |
| Clock Channel | Maximum Settling Time | Tested Value | Pass |
| 1 | 20 nsec |  |  |
| 2 | 20 nsec |  |  |
| 3 | 20 nsec |  |  |
| 4 | 20 nsec |  |  |
| 5 | 20 nsec |  |  |
| 6 | 20 nsec |  |  |
| 7 | 20 nsec |  |  |
| 8 | 20 nsec |  |  |
| 9 | 20 nsec |  |  |
| 10 | 20 nsec |  |  |
| 11 | 20 nsec |  |  |
| 12 | 20 nsec |  |  |
| 13 | 20 nsec |  |  |
| 14 | 20 nsec |  |  |
| 15 | 20 nsec |  |  |
| 16 | 20 nsec |  |  |
| 17 | 20 nsec |  |  |
| 18 | 20 nsec |  |  |
| 19 | 20 nsec |  |  |
| 20 | 20 nsec |  |  |
| 21 | 20 nsec |  |  |
| 22 | 20 nsec |  |  |
| 23 | 20 nsec |  |  |
| 24 | 20 nsec |  |  |
| 25 | 20 nsec |  |  |
| 26 | 20 nsec |  |  |
| 27 | 20 nsec |  |  |
| 28 | 20 nsec |  |  |
| 29 | 20 nsec |  |  |
| 30 | 20 nsec |  |  |

ADC Offset Error

Offset Error

|  |  |  |  |
| --- | --- | --- | --- |
| Analog Signal Channel | Maximum Offset Error | Tested Value | Pass |
| 1 | ±1.5 LSB |  |  |
| 2 | ±1.5 LSB |  |  |
| 3 | ±1.5 LSB |  |  |
| 4 | ±1.5 LSB |  |  |
| 5 | ±1.5 LSB |  |  |
| 6 | ±1.5 LSB |  |  |
| 7 | ±1.5 LSB |  |  |
| 8 | ±1.5 LSB |  |  |

ADC missing codes

Missing Codes

|  |  |  |  |
| --- | --- | --- | --- |
| Analog Signal Channel | Missing Codes Allowed | Tested Value | Pass |
| 1 | No |  |  |
| 2 | No |  |  |
| 3 | No |  |  |
| 4 | No |  |  |
| 5 | No |  |  |
| 6 | No |  |  |
| 7 | No |  |  |
| 8 | No |  |  |

ADC/Signal Chain Noise

Maximum RMS Noise

|  |  |  |  |
| --- | --- | --- | --- |
| Analog Signal Channel | Maximum RMS Noise Over All ADC Conversions | Tested Value | Pass |
| 1 | 1 LSB |  |  |
| 2 | 1 LSB |  |  |
| 3 | 1 LSB |  |  |
| 4 | 1 LSB |  |  |
| 5 | 1 LSB |  |  |
| 6 | 1 LSB |  |  |
| 7 | 1 LSB |  |  |
| 8 | 1 LSB |  |  |

ADC DNL

Maximum Differential Non-Linearity

|  |  |  |  |
| --- | --- | --- | --- |
| Analog Signal Channel | Maximum DNL | Tested Value | Pass |
| 1 | 1 LSB |  |  |
| 2 | 1 LSB |  |  |
| 3 | 1 LSB |  |  |
| 4 | 1 LSB |  |  |
| 5 | 1 LSB |  |  |
| 6 | 1 LSB |  |  |
| 7 | 1 LSB |  |  |
| 8 | 1 LSB |  |  |

# References

1 Bill Jasper, “Practical Telecom DAC Testing”, Test Edge Inc., pp 7-8.

2 Joey Doernberg, Hae-Seung Lee, and David A. Hodges, “Full-Speed Testing of A/D Converters”, *IEEE Journal of Solid-State Circuits* (December 1984): 820-827.

3 Application Note, “Histogram Testing Determines DNL and INL Errors”, Maxim Integrated, 18 June 2003.