Meeting Notes February 14,2013

Attendees: Stephen Kaye, A. N. Ramaprakash, Pravin Chordia, Mahesh Burse

**Minutes**

* ADC layout was shown and discussed
* IUCAA has tested the ADC at 100 kHz and has gotten data from the ADC
* More extensive tests need to be run on the ADC and will be done
* The ADC will also be run at higher rates – goal of 1 MHz
* Layout for the integrator and integrating capacitors was shown and discussed
* The layout shows through-hole capacitors on the top side of the board. These are the polypropylene capacitors
* The capacitors in parallel are on the bottom side of the board.
* Each of these capacitors will be tested and the best type will be chosen
* Design note on compensating for capacitive load was discussed
* The topology in the schematic for the bias voltage does not look like the correct topology from the design note. This will be looked into
* The bias voltage has not been tested, so there is no data on performance of bias voltage
* Schedule for work from IUCAA is in development. The hope is to have something by next week.
* Ram will be visiting JPL next week. If there is time in everyone’s schedule, we will get together to talk about schedule and other concerns
* Caltech is in process of writing up the pre-amplifier design document. The interface to the video board is not done yet, but is in progress
* Caltech is in process of writing up a testing document

**Action Items**

 **Caltech**

* + Caltech will finish and post the document describing performance of pre-amp and ideas for a fully digital CDS.
	+ Caltech will provide a document describing test method for integration capacitor and coupling capacitor signal memory
	+ Caltech will continue work on a testing document which will describe tests to be performed on the analog card. Document will include spaces for test results, and provide acceptable ranges for test results.

**IUCAA**

* + IUCAA will provide a schedule document describing what they intend to accomplish and by what date. The milestones will also include dates for reviews of designs and reviews of performance tests.
	+ Will test ADC at higher sample rates
	+ Will look into topology of bias amplifier and the capacitive load compensation