Meeting Notes February 4,2013

Attendees: Stephen Kaye, Roger Smith, A. N. Ramaprakash, Pravin Chordia, Mahesh Burse

**Minutes**

* Analog board questions and concerns were discussed
* AD8099 op-amps have been used by IUCAA with good results
* Two integration capacitors in parallel are for two different types of capacitors which will be tested for best performance
* Caltech recommended a test for integration capacitors which will be written up and posted on twiki
* Bypass capacitors are used at each op-amp power pin. Orcad hides these details due to hierarchical design flow.
* Trace width for analog board is 6 mils to 8 mils. Caltech suggests 10mils to 12 mils especially for power pin traces
* A/D converter anti-aliasing filters have too high a corner frequency for 1 MHz operation. Thought needs to go into what corner frequency we should use.
* Extra resistor in buffer amplifier output path was recommended by Analog Devices for driving capacitive loads. IUCAA will email application note to Caltech.
* Since another layout will happen for the new packaging, we agreed that a red line schematic showing the which components will not be included in next version will be done
* Caltech has a design for a pre-amp near the CCD. A pre-amp on the analog board will not be needed.

**Action Items**

 **Caltech**

* + Caltech will provide a document describing performance of pre-amp and ideas for a fully digital CDS.
	+ Caltech will provide a document describing test method for integration capacitor and coupling capacitor signal memory
	+ Caltech will provide a testing document which will describe tests to be performed on analog card. Document will include spaces for test results, and provide acceptable ranges for test results.

**IUCAA**

* + IUCAA will provide a schedule document describing what they intend to accomplish and by what date. The milestones will also include dates for reviews of designs and reviews of performance tests. This document will be revised by email and will be discussed when Ram visits Caltech.