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| Caltech |
| Testing and Tuning CCDs for WaSP |
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**Testing and Tuning CCDs for WaSP**

1.1, February 9, 2016

Caltech

# To Do List

1. Single-sided video waveform checkout

Take data for each side. Subtract digitally. Compare to oscillosope mode.

Estimate common mode rejection

Take data for all 4 channels

1. Reset feedthrough

Document amplitude of reset feedthrough voltage

Clock feedthrough

1. Adjust reset drain level and effect on reset feedthrough amplitude
2. Validate on chip clamp operation (TGA and TGD)…
3. X Survey all of the clocks for features
4. X Multiple exact same states of the parallel clock

X Positive single sided, negative single sided, both, or neither flag. Put in preprocessing software.

# To Do Results/Procedure

## Video Waveform Check

Oscilloscope mode was used for amplifier 5. Three horizontal raw plots were taken. The first had both the signal output and the dummy output enabled. The second had the dummy side grounded so that only the signal side was digitized. The third had the signal side grounded so that only the dummy side was digitized.

## Reset Feedthrough

This test looks at the height of the reset clock feedthrough on the video signal. This height can be affected by the low clock level of the reset pulse, the high clock level of the reset pulse, and the voltage level of the reset drain. Each of these voltages is supplied by the bias card in the WaSP controller (slot 8). For each of these voltages, the voltage is changed in 1 V steps and raw data is collected on each of the raw ADC channels 5-8.

The script should use reverse clocking so that we are not affected by temperature and this test can be done at any time regardless of the state of the dewar. Also, we need to ground the negative side of the preamplifier so that we are looking at a single sided video signal. Otherwise, the feedthrough will be mostly eliminated due to its common mode nature. Therefore, the software preprocessor should set the following:

#DEFINE \_SER\_CLOCKING\_DIR REVERSE

#DEFINE \_HOLD\_BLACK\_LEVEL\_CLAMP NEG

#DEFINE \_LINES\_PER\_TAP 10

#DEFINE \_PIXELS\_PER\_TAP 110

#DEFINE \_RAW\_ENABLE 1

#DEFINE \_RAW\_STARTLINE 0

#DEFINE \_RAW\_ENDLINE 9

#DEFINE \_RAW\_STARTPIXEL 0

#DEFINE \_RAW\_SAMPLES 10240

#DEFINE \_RAW\_SELECT 4

Everything else in the wasp.def file remains at the default setting.

### Low reset clock level

The reset drain is set to 18 V

The reset gate high level is set to 12 V

The reset gate low level is set to 0 V

Repeat the following until reset gate low is 11V

Save raw data from channels 5, 6, 7, and 8.

Increase reset gate low level by 1V and apply

### High reset clock level

The reset drain is set to 18 V

The reset gate high level is set to 12 V

The reset gate low level is set to 0 V

Repeat the following until reset gate high is 3 V

Save raw data from channels 5, 6, 7, and 8.

Decrease reset gate high level by 1V and apply

### Reset drain level

The reset drain is set to 18 V

The reset gate high level is set to 12 V

The reset gate low level is set to 0 V

Repeat the following until reset drain is 21 V

Save raw data from channels 5, 6, 7, and 8

Increase reset drain level by 1 V and apply

Set reset drain to 18 V

Repeat the following until reset drain is 16 V

Save raw data from channels 5, 6, 7, and 8

Decrease reset drain level by 1 V and apply

## Transfer Gate Feedthrough (or On-Chip TG Clamp Validation)

This test looks at the height of the transfer gate clock feedthrough on the video signal. This height can be affected by the low clock level of the transfer gate pulse, the high clock level of the transfer pulse, and the voltage level of the reset drain. The transfer gate clock voltages are provided by a WaSP clock board (slot 9, channel 1) and the reset drain voltage is supplied by the bias card in the WaSP controller (slot 8, channels 5, 6, 7, and 11). For each of these voltages, the voltage is changed in 1 V steps and raw data is collected on each of the raw ADC channels 5-8.

The transfer gate voltages are controlled by two Constants, TG\_low and TG\_high for the low clock level and high clock level, respectively. Each time a new clock level is generated, the whole acf must be reloaded.

The script should use reverse clocking so that we are not affected by temperature and this test can be done at any time regardless of the state of the dewar. Also, we need to ground the negative side of the preamplifier so that we are looking at a single sided video signal. Otherwise, the feedthrough will be mostly eliminated due to its common mode nature. Therefore, the software preprocessor should set the following:

#DEFINE \_SER\_CLOCKING\_DIR REVERSE

#DEFINE \_HOLD\_BLACK\_LEVEL\_CLAMP NEG

#DEFINE \_RAW\_ENABLE 1

#DEFINE \_RAW\_STARTLINE 2000

#DEFINE \_RAW\_ENDLINE 2050

#DEFINE \_RAW\_STARTPIXEL 0

#DEFINE \_RAW\_SAMPLES 10240

#DEFINE \_RAW\_SELECT 4

Everything else in the wasp.def file remains at the default setting.

### TG\_low clock level

The reset drain is set to 18 V

TG\_high is set to 10 V

TG\_low is set to 0 V

Repeat the following until TG\_low is 8 V

Save raw data from channels 5, 6, 7, and 8.

Increase reset gate low level by 1V and apply

### TG\_high clock level

The reset drain is set to 18 V

TG\_high is set to 10 V

TG\_low is set to 0 V

Repeat the following until TG\_high is 5 V

Save raw data from channels 5, 6, 7, and 8.

Decrease reset gate high level by 1V

### Reset drain level

The reset drain is set to 18 V

The reset gate high level is set to 12 V

The reset gate low level is set to 0 V

Repeat the following until reset drain is 21 V

Save raw data from channels 5, 6, 7, and 8

Increase reset drain level by 1 V

Set reset drain to 18 V

Repeat the following until reset drain is 16 V

Save raw data from channels 5, 6, 7, and 8

Decrease reset drain level by 1 V

## Reset Drain Level Adjustment

## Parallel Clock Glitches

One idea about the parallel clock is that the levels were being set to the same voltage multiple times during the charge transfer. The multiple settings to the same clock were removed from the configuration file, but the glitches remained. It is indeed the inter-phase capacitance that is the problem. To double check, multiple exact states can be written with no clock levels changed and see if the glitches go away as a positive sign that writing the same level twice doesn’t glitch the clock.

Multiples of the sample clock state was written, and no glitches occurred when writing the same exact state. Again, this points to inter-phase capacitance as the reason for parallel clock glitches.

This clock glitch does not appear on the serial clocks.

# Introduction

After the control electronics for the focal plane CCDs has been characterized, the CCDs themselves must be characterized. Many parameters can be adjusted (e.g. Clock levels, bias levels, and clock overlap) to improve the performance of the CCDs. This document outlines the tests which will be performed to characterize the CCDs along with the parameters to adjust to optimize the performance of the CCDs for ZTF. With a large mosaic such as ZTF, this process must be automated in order to efficiently arrive at the final configuration of the clocks, biases, and waveforms.

# Photon Transfer Curve

A photon transfer curve can be extremely useful in determining many characteristics of a CCD. In the case of ZTF, an illuminator board will be mounted at the front face of the cryostat. This illuminator board will be used as the source for photon transfer curves for the CCDs.

The LEDs will be programmed to turn on for a specified amount of time, and then notify the controllers to read out the CCDs. We will collect three images for each light level and use for the plotting of the PTC.

We can use the trigger output from the controllers as the gating for the illuminator board. The output signal from the controller is the same signal that will be used for the shutter. This signal will be input into the Arduino which controls the illuminator board. From this, we can measure the gain, the read noise, the linearity, the full well, and the dynamic range of the CCD.

## Gain (e-/DN)

The gain can be changed by changing the preamplifier setting of the A/D Module, but a loss of dynamic range would occur. Therefore, the gain will be measured, but not affected.

## Read Noise

The read noise can be improved with a slower readout. It can also perhaps be improved with shorter cables. This result will be compared with the result of the VIB amplifier test, the published CCD amplifier noise result, and the A/D Module noise test result. This read noise should be equal to those contributions added in quadrature.

## Full Well

The full well can be affected by the voltage level on the parallel and serial clocks. The measurement should be compared with the published test results for each specific CCD to determine if the full well is acceptable.

## Dynamic Range

The dynamic range can be increased or decreased due to the gain in the preamplifier on the A/D Module. Compare against a specification for the dynamic range. How can we affect this other than electronic gains through the signal chain?

## Linearity

# Charge Transfer Efficiency

Use 55Fe to test this? Or will we use an illumination and several extra transfers?

## Parallel

## Serial

# Quantum Efficiency

Need an optical setup with a known wavelength

# Crosstalk

# Dark Current

# Clock Induced Charge