Keck Adaptive Optics Note 718

Keck Next Generation Adaptive Optics
LGS and NGS Wavefront Sensor Cameras

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1. Introduction

This note describes the baseline wavefront sensor cameras for the laser guide star (LGS) and natural guide star (NGS) wavefront sensors in the Next Generation Adaptive Optics (NGAO) system at the W. M. Keck Observatory (WMKO).

2. Background

The LGS and NGS wavefront sensors for the NGAO system require Shack Hartmann wavefront sensors with ~63 x 63 subapertures. For LGS operation the lasers will be center projected, so LGS image perspective elongation is not considered significant over the offset distance to the outermost subaperture of 5.36 m (17 cm subaperture spacing x (63/2)). Sufficient sensitivity and linearity for local tilt across the subaperture, even with the small amount of elongation present, can be obtained by allocating 4 x 4 pixels per subaperture. A CCD with 256 x 256 pixels will provide a sufficient number of subapertures. A separate WMKO project (Adkins, 2010, included as appendix A to this document) has been developing low noise, high performance AO imagers in collaboration with the Lincoln Laboratory of the Massachusetts Institute of Technology (MIT/LL).

Most recently, through collaboration among WMKO, the Starfire Optical Range (SOR) operated by the Air Force Research Laboratory at Kirtland Air Force Base, and the Thirty Meter Telescope project a shared wafer run carrying designs developed by MIT/LL for SOR and WMKO has been started. This wafer run includes a design for a 256 x 256 pixel AO imager designated the CCID-74, designed by MIT/LL in response to the requirements developed by WMKO. The final requirements for this detector based on the completed design are given in appendix A.

At the same time, in collaboration with MIT/LL and the TMT, WMKO has led the development of a novel CCD for wavefront sensing called the polar coordinate detector which addresses the problem of LGS image perspective elongation on an extremely large telescope, where the effects on wavefront sensing performance are much more significant. The polar coordinate detector is the baseline LGS wavefront sensor for the TMT, and details of the polar coordinate detector design are given in Adkins (2007). A customized 128 channel readout system with the readout electronics located at the focal plane is planned for the polar coordinate detector (Adkins, 2008b). This readout system is also planned for use with the CCID-74 in a 64 channel configuration as the NGS wavefront sensor camera for the TMT.

3. NGAO LGS and NGS Wavefront Sensor Cameras

The combination of the CCID-74 and the 64 channel version of the readout system with focal plane electronics as planned for the TMT are proposed as the baseline for the NGAO LGS and

NGS wavefront sensor cameras. A preliminary configuration and dimensions for the CCID-74 camera are shown in Figure 1.

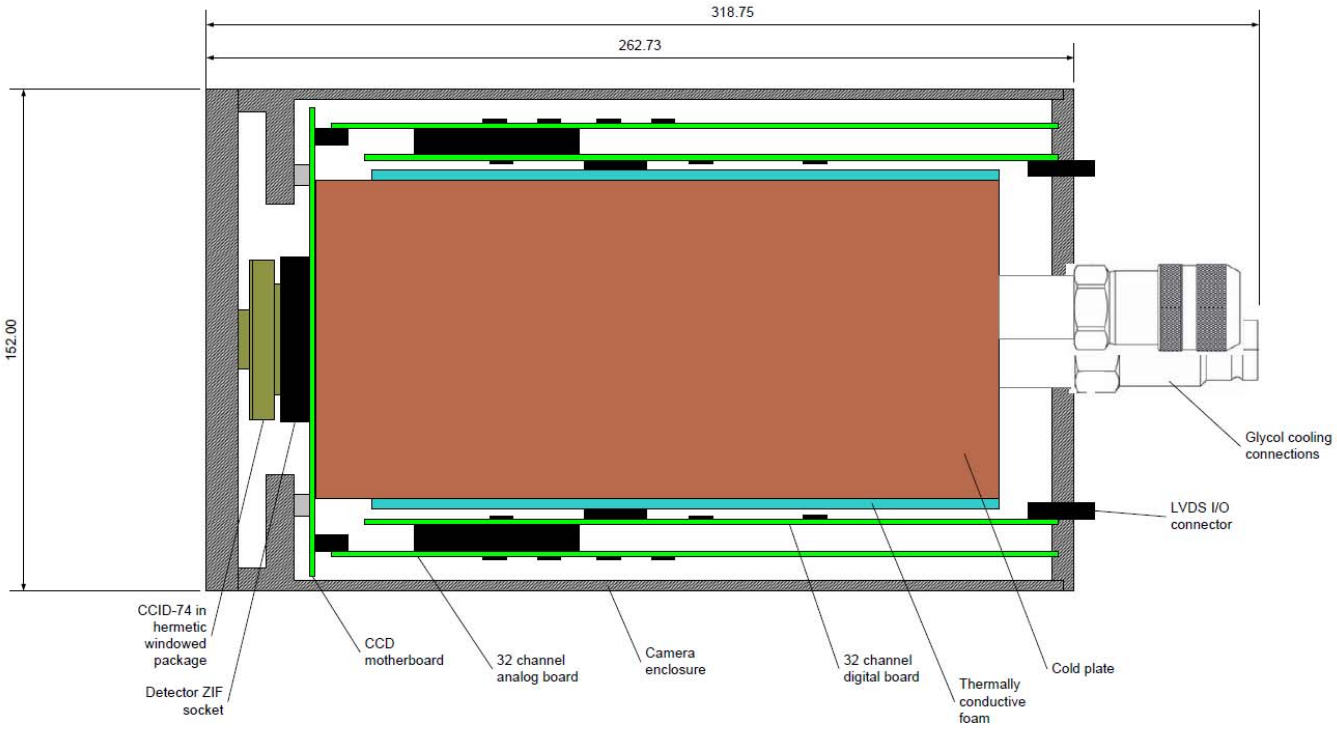

Figure 1: CCID-74 Camera
Cross section view. Not visible: power connector and details of cold finger and mounting of CCD for thermal stability.

The CCID-74 is packaged in a 131 pin hermetic windowed package with a two stage thermoelectric cooler (TEC). The CCID-74 camera and the camera for the polar coordinate detector share a common overall envelope. The polar coordinate detector package will also be a hermetic package with a window and a two stage TEC, but will be larger than the CCID-74 with 286 pins. The CCID-74 camera will use two of the 32 channel analog and digital board pairs to read out the detector using 64 video channels.

For the CCID-74 camera two pairs of the analog and digital boards plug-in to the CCD motherboard as shown in Figure 1. The higher power dissipation digital board will be cooled by a cold plate with the thermal connection made using thermally conductive foam pads (Bergquist Gap Pad). The cold plate will also cool the hot side of the TEC on the CCD.

Each of the digital boards has a low voltage digital signaling (LVDS) interface connector (~44 pins), and the camera also has a power connector for DC power input, and power to the TEC. Closed loop operation of the TEC is supported by a temperature sensor mounted in the CCID-74 package.

The LVDS connectors and the power connector interface the camera to a 1U high EIA 19 inch rack mounted interface controller module (see Adkins, 2008b). The LVDS cables are

limited to a maximum length of ~3 m. The interface controller is designed for mounting in a sealed enclosure cooled by a liquid to air heat exchanger.

4. Interfaces

The overall dimensions of the camera enclosure are 152 mm wide, 152 mm high, and ~263 mm deep not including the electrical and cooling connections (see Figure 1). Details of mounting for the camera and its interface to the NGAO LGS and NGS assemblies will be determined during the NGAO detailed design phase. The front plate of the enclosure can be customized as needed to provide the required interface to the wavefront sensor optics.

The camera head is cooled by a cold plate that uses a fluid (glycol based) coolant. The camera head will dissipate no more than 17 W (Adkins, 2008a). The interface controller is designed for forced air cooling, and will dissipate ~30 W.

As discussed in Adkins (2008b) the interface controller uses the serial front panel data port (sFPDP) protocol over optical fiber to communicate with the AO system's real time wavefront controller. The CCID-74 camera will require two, 2.5 Gbps optical links at 850 nm with 50/62.5 μm multimode fiber for distances up to 500 m. Each link consists of a transmit and receive fiber pair with a duplex LC style connector.

5. Summary specifications

The specifications for the CCID-74 camera are summarized in Table 1.

Table 1: CCID-74 Camera Specifications

Parameter	***Min.***	***Typ.***	***Max.***	***Units***	***Notes***
Active area	-	256 x 256	-	pixels	1
Pixel pitch	-	21	-	μm	1
Wavelength range	400	-	1000	nm	1
Frame rate	-	-	2000	Hz	1
Data format	-	TBS	-	-	
Camera					
Signal connector	-	TBS	-	-	2
Power connector	-	TBS	-	-	3
Cooling connections	-	FS-251-4	-	-	4
Coolant requirements					
Supply temperature	-5	0	7	ºC	5
Coolant pressure	-	45	100	psig	
Flow rate	TBS	4	-	l/min	
Pressure drop	-	6	TBS	psi	
Power dissipation	14	-	17	W	
Overall dimensions	-	152 x 152 x 263	TBS	mm	6
Interface controller					
Camera connectors					
Digital I/O	-	TBS	-	-	2
Power	-	TBS	-	-	3
Data connectors	-	Type LC	-	-	7
Control connector	-	RJ-45	-	-	8
Power requirements					
Voltage	108	120	132	Vac	
Current	-	1	-	Amperes	
Frequency	57	60	63	Hz	
Power connector	-	IEC C14	-		9
Power dissipation	24	-	30	W	

Notes:

1. Determined by CCID-74 detector characteristics, see appendix A for the CCID-74 specifications.
2. Two LVDS signal connectors with ~ 44 pins meeting the requirements of ANSI/TIA/EIA-644-A.
3. One 38999 series IV connector with pin contacts, pin count TBD.
4. Parker-Hannifin ¼ inch FS series quick disconnect fittings, male (FS-251-4MP) for supply to the camera, female (FS-251-4FP) for return to the external cooling system.
5. Coolant is 50% by volume Dowtherm SR1 with water.
6. Width x height x depth, mounting details TBS.
7. Two duplex LC connectors, one for each of 32 channels of video output from the camera.
8. 1000Base-T conforming to IEEE 802.3ab. Control protocol based on TCP/IP format TBD.
9. IEC C14 style panel mounted male inlet with connector retaining spring.

6. References

1. Adkins, S. (2007, October 14). *Polar Coordinate Detector Final Draft Specification.* Waimea, HI: W. M. Keck Observatory.

2. Adkins, S. (2008, July 30). *Thirty Meter Telescope project, polar coordinate detector thermal considerations*. Waimea, HI: W. M. Keck Observatory.

3. Adkins, S. (2008, October 23). *Polar coordinate detector readout system.* Waimea, HI: W. M. Keck Observatory.

4. Adkins, S. (2010, February 25). *Requirements for a 256 x 256 Pixel Low Noise Detector*. Waimea, HI: W. M. Keck Observatory.

Appendix A: Requirements for the CCID-74

The CCID-74 requirements document is included following this page. This document should be cited as:

> Adkins, S. (2010, February 25). *Requirements for a 256 x 256 Pixel Low Noise Detector*. Waimea, HI: W. M. Keck Observatory.

W. M. KECK OBSERVATORY

Next Generation Optical Detectors for Wavefront Sensing
Requirements for the CCID-74, a 256 x 256 Pixel Low Noise Detector

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INTRODUCTION

This document describes the requirements for a larger version of the low noise detector known as the CCID-56b developed in collaboration with the Lincoln Laboratory of the Massachusetts Institute of Technology (MIT/LL) as part of a project led by the W. M. Keck Observatory and funded by the Adaptive Optics Development Program (AODP).

At the present time we have identified at least three parties interested in a larger version of the CCID-56b for both adaptive optics (AO) wavefront sensing and high speed or very low noise imaging applications. This document gives the requirements for this larger device, designated the CCID-74. These requirements were developed after careful consideration of several design trade-offs and taking into account the needs of the potential users.

ARCHITECTURE

The CCID-74 is based on the architecture of the CCID-56b/d, shown in Figure 1. The CCID-56b/d is a 160 x 160 pixel split frame transfer, backside illuminated CCD imager with 20 video outputs. The device has a 45 µm substrate with a mid-band optimized anti-reflection (AR) coating. The output amplifiers employ an output structure based on a planar JFET. Off-chip source follower buffers are provided for each video output to lower the detector output impedance.

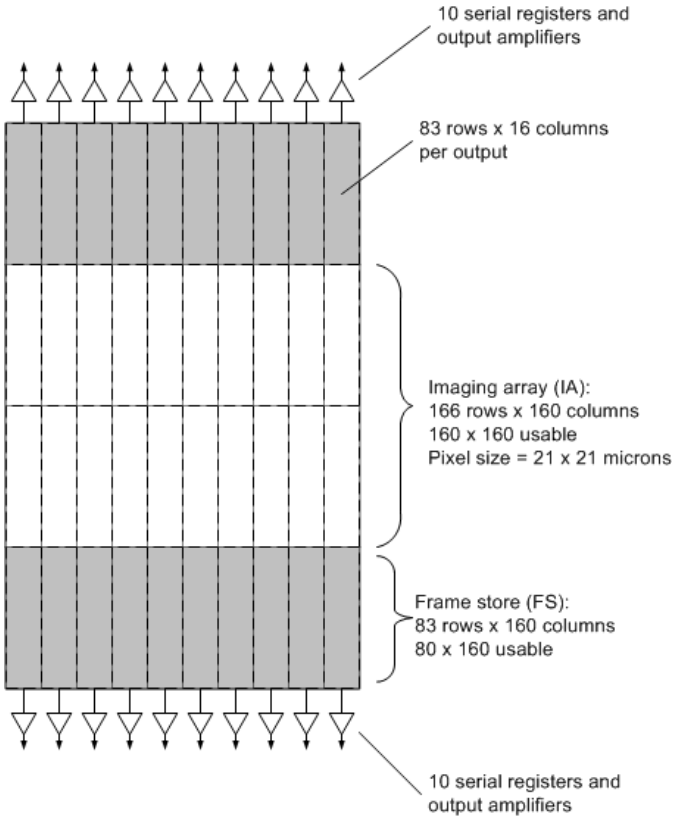

Figure 1: CCID-56b/d imager architecture

The CCID-56b/d design has also been used as the basis for a second 160 x 160 pixel imager, the CCID-66 which has been fabricated on a PanSTARRS orthogonal transfer array (OTA) development lot. The CCID-66 is identical to the CCID-56b with the exception of the video output structure which incorporates a second amplifier stage on each output, allowing much higher pixel read out frequencies and correspondingly higher frame rates. The CCID-56b was designed with a single stage amplifier because of concern that the second stage might increase the read noise, but testing has shown that in fact there is little or no increase in read noise with the second stage of amplification.

The most recent test results from the testing of a CCID-66 based camera system built by SciMeasure for the Starfire Optical Range (SOR) are summarized in Table 1. The results shown in this table are for data obtained by Robert Johnson (SOR) and John Wynia (Boeing) from camera #53 (blue figures) and SciMeasure (black figures). The first read noise column shows the average read noise for the best contiguous outputs (2 or more), and the second column indicates the minimum and maximum read noise for each of the 20 outputs. We have observed some variation in read noise between the upper and lower halves of the imager, and from output to output. The variation between the upper and lower halves is attributed to the sensitivity of the JFET output structure to small mask misalignments. The JFET output structure is more sensitive to misalignments than the rest of the CCD or a conventional MOSFET transistor output structure. In the CCID-66 the upper and lower halves of the layout were created by rotating one half of the layout 180 degrees. This causes mask misalignment to move features in the opposite direction between halves of the device, affecting the JFET performance.

Pixel clock rate, MHz	Best average read noise, e^-	Min./Max. read noise, e^-	Frame rate, Hz (160 x 160)	Frame rate, Hz (96 x 96)	Frame rate, Hz (96 x 48, TAGR)
0.5	1.3	-	358*	-	-
1	1.67	-	710*	-	-
2.38	2.0	1.8/4.1	1,653*	-	-
2.94	2.8	2.2/4/4	2,023*	-	-
3.85	4.6	3.5/5.8	2,607*	3,940*	5,010*

* = interleaved

Table 1: CCID-66 test results, 3.85 MHz row transfer rate

The frame rates shown in Table 1 were obtained using an interleaved readout mode, where row transfers are interleaved with serial register clocking. Each row is transferred to the frame store as soon as the last pixel from the previous row enters the prescan pixel segment of the serial register. This eliminates the repeated overhead associated with clearing and filling the ADC pipeline and prescan pixels, improving the readout efficiency. The interleaving does not appear to increase the readout noise. The TAGR (throw away guard rows) mode shown in the 96 x 48 table column is used with the SOR quad cell Shack Hartmann wavefront sensors which use 24 x 24 subapertures over 96 x 96 pixels at the center of the CCID-66. There are two unused rows between each row of subapertures, so these rows are both clocked into the frame store and then clocked out of the serial register at the maximum possible speed (6 readout system clocks per pixel).

It has been found that the planar JFET output structure design appears to allow more reset feedthru than is usual with the more conventional MOSFET output structures. By holding the extra clock phase

connection to the last pixel in the serial register low and filtering it with an external capacitor this reset feedthru has been significantly reduced at the expense of the summing well feature on the serial registers. Based on the results of testing at SciMeasure and by MIT/LL, the CCID-74 and other new devices using the planar JFET output structure will incorporate a dual output gate structure to provide a reduction in reset feedthru without losing the summing well feature.

CCID-74 Architecture

The architecture of the CCID-74 is shown Figure 3. The device is a 256 x 256 pixel split frame transfer imager with 64 video outputs. The imager and frame store parallel clocks are three phase, and the serial registers are two phase.

The frame store, serial registers and output amplifiers are provided with a light shield, and in order to ensure that the entire active area of the device remains un-obscured by the light shield, extra rows and columns are provided as illustrated in Figure 2. Typically 3 extra rows are provided on each side of the imager array (IA) and 3 extra columns of pixels are provided at each end of the IA. These extra rows and columns are also provided in the two halves of the frame store (FS). In the row transfer direction these extra rows must be transferred out of the IA and into the FS. The extra rows are the first rows to reach the serial register and here they are simply transferred through the serial register in the row transfer direction to a dump drain, eliminating the overhead that would otherwise be incurred by clocking these extra rows out of the serial register. The extra columns on each side of the FS are connected directly to the dump drain instead of adding extra pixels to the serial register.

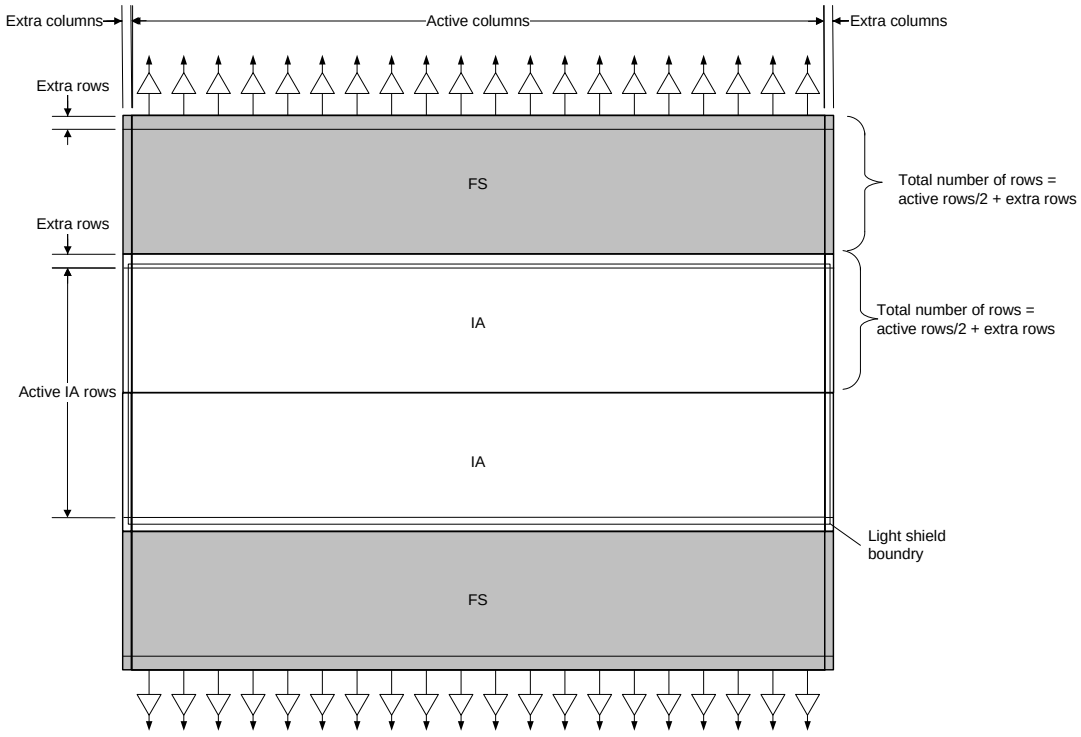

Figure 2: Light shield with extra rows and columns

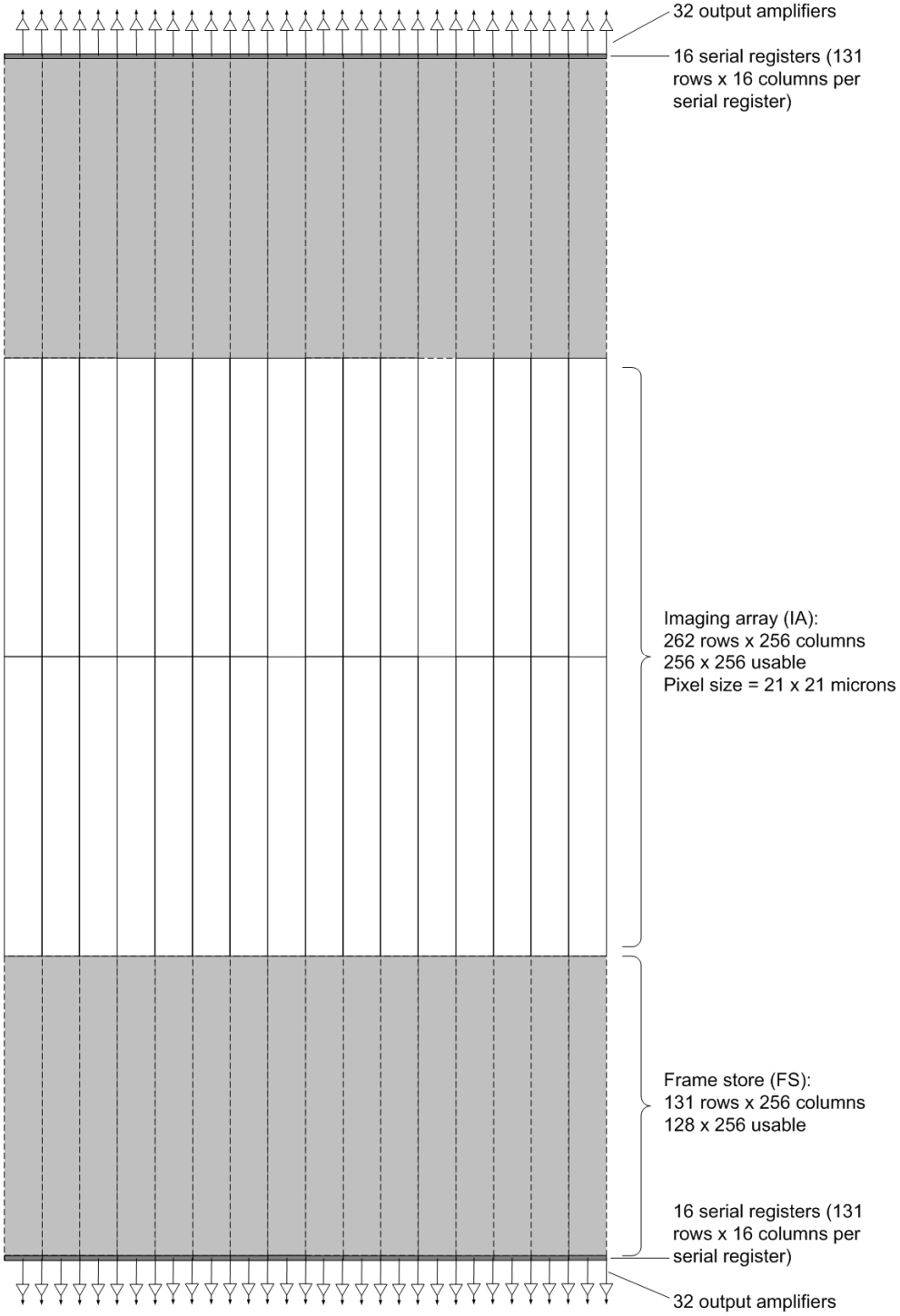

Figure 3: 256 x 256 imager architecture

CCID-74 Serial Register Design

The CCID-56b/d and CCID-66 use a three phase serial register. This was the standard at the time these devices were designed. However, a two phase serial register has been developed by MIT/LL and implemented on the Pan-STARRS OTA devices (CCID-58). The two phase serial register improves the charge transfer efficiency in the serial register, allowing higher serial clock rates, and reduces the clock feedthru in the video output. Because of these advantages the CCID-74 will use a two phase serial register.

For some applications the goal is to obtain the lowest possible read noise, with frame rate being a secondary consideration. For these applications it would be desirable for reasons of interconnect complexity and cost to use a smaller number of read out channels. For the CCID-74, offering the option of reading the device out through 32 channels means that the device would match a SciMeasure read out system configuration with 8 of the 4 channel video boards, the largest number of video boards currently supported in a single system (one EIA 19 inch rack mount of 3U height).

The trade-off between pixel read out frequency and noise makes it appropriate to also offer a 64 channel read out mode, even though this leads to the need to either synchronize two SciMeasure read out systems, or to implement another solution for 64 channel read out mode. The 64 channel read out mode will be applicable to laser guide star (LGS) wavefront sensing for the WMKO Next Generation AO system (NGAO) where a high frame rate will be required, and where the relatively bright LGS images will make somewhat higher read noise levels due to the wider read out system bandwidth acceptable. The 64 channel mode will also permit the slowest possible pixel read out rate for lower frame rate applications such as NGS wavefront sensing for the Thirty Meter Telescope (TMT) project and for the NGAO system.

MIT/LL has considered the requirement for both 32 and 64 channel read out modes, and has arrived at a novel multiplexed serial register to support both read out modes. This serial register is illustrated in Figure 4. Note that this is a simplified illustration; details such as the dual output gates at the last pixel of each serial register have been omitted.

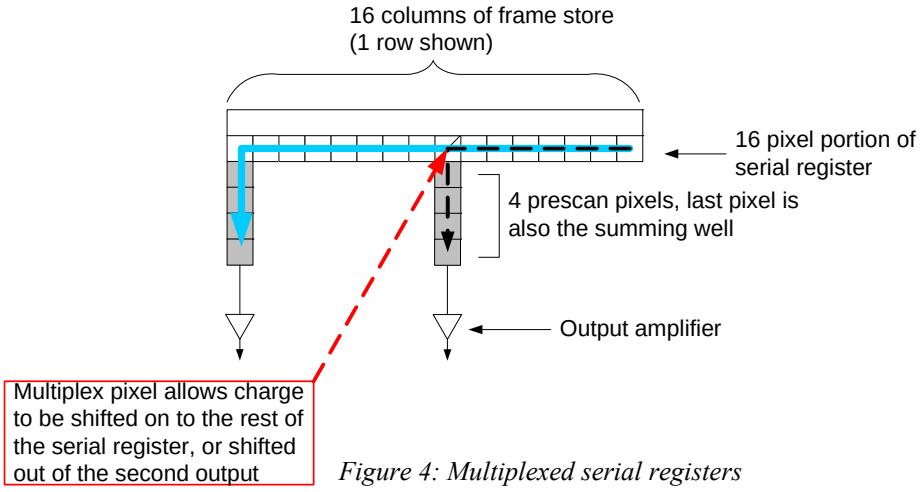

Figure 4: Multiplexed serial registers

Every 16 columns of the device are provided with a two phase serial register. The eighth pixel in the portion of the serial register at the end of the frame store columns has a multiplexer created by two barrier structures each controlled by fixed voltages. One barrier blocks charge from continuing to be shifted into the left in Figure 4 into the ninth and following pixels of the remaining portion of the serial register. When this barrier is opened charge is shifted through the eighth pixel and into the left hand most serial register segment (the path of the charge indicated by the blue line) and read out through the corresponding output amplifier.

The other barrier structure blocks charge from being shifted into the prescan pixels connected to the eighth pixel in the serial register. When this barrier is opened and the other barrier closed, the first eight pixels are shifted out through the second set of prescan pixels (the path of the charge indicated by the black dashed line) and read out through the second output amplifier. The device signal that controls the barrier in the multiplex pixel for charge travelling along the serial register, that is parallel to the imager and frame store rows, is called MUXR for multiplex row [direction], and the signal that controls the barrier for charge travelling out of the multiplex pixel and into the prescan pixels of the video output at the multiplex pixel is called MUXC for multiplex column [direction].

In this way either two sets of 8 pixels from each row in a 16 pixel column of the frame store are read out through two output amplifiers, or 16 pixels from each row are read out through a single output amplifier. This structure is repeated for the remaining active columns on each half of the frame store (256 columns total), resulting in 16 serial register segments multiplexed to two output amplifiers for a total of 32 amplifiers on each half of the frame store.

Additional Serial Register Features

A dump drain is provided for the serial register allowing a row of charge to be shifted in the row transfer direction through the serial register into the drain rather than having to be clocked out through the serial register in order to dump the charge of an unwanted row.

Based on the experience with read out clock feedthru on the CCID-56b and CCID-66 the serial register will have a dual output gate. This will allow the second gate to function as an isolation and filtering gate, an approach that has been shown to significantly reduce clock feedthru. Also, on the last pixel of the serial register a separate phase line allows the last pixel to be operated as a summing well.

Common Design Assumptions

For risk reduction we have kept a number of the design parameters constant between the CCID-66 and the CCID-74. The following design parameters have been maintained in common with the CCID-66:

- Split frame transfer design
- Planar JFET output structure for each video output
- A single bias input for all outputs on each half of the frame store
- 21 μm square pixels of similar size
- Fabricated on high resistivity silicon, 75 μm nominal substrate thickness

Planar JFET Output Structure

The planar JFET output structure uses a p-channel JFET transistor constructed directly over the sense node at the end of the serial register. This configuration results in reduced capacitance at the transistor gate, and the design provides higher responsivity and lower noise due to the characteristics of the JFET. The planar JFET output structure provides approximately two times the responsivity of the MOSFET based output structure that is normally employed in MIT/LL designs. This higher responsivity results in a higher output voltage from the output amplifier, improving the signal to noise ratio (SNR) by a similar factor.

The main goal of the CCID-56b design was to exploit the low read noise possible with the planar JFET output structure. For this reason each output incorporates only a single stage of amplification on the device. This amplifier has limited ability to drive the capacitive load presented by the gate of the n-channel JFET that is mounted on the ceramic carrier in the device package to provide an output source follower for each video output. In the CCID-56b the U309 transistor that is normally used in MIT/LL device packages was changed to a 2N4416. While this improved performance the source to drain resistance of the 2N4416 limits the output slew rate, resulting in a maximum pixel read out frequency of ~1.5 MHz. The termination resistors at the read out system end of the video signal coaxial cables also had to be increased in value which reduced the match to the cable impedance and may have slightly increased the read out noise.

In the CCID-66 a second stage of amplification on the device for each video output allows use of the standard U309, and results from CCID-66 testing (Table 1) have demonstrated a 3.85 MHz pixel read out frequency.

Read out Process

Referring to Figure 1, the read out process for a split frame transfer CCD consists of first transferring all of the rows from each half of the imager array to the corresponding frame store. Once this process is completed integration of charge resumes in the imager array for the next exposure while the frame store is transferred one row at a time to the serial registers. The pixel values are then read out one at a time by shifting the charge along the serial register to the output amplifier. By dividing the serial register into subsections, each with its own output amplifier, the readout process can be made faster while maintaining the same pixel read out frequency, which allows a lower noise level to be achieved for a given frame rate.

For example, the CCID-56b, illustrated in Figure 1, has 160 pixels in each row, and 10 serial registers and output amplifiers on each half of the frame store. This means that each serial register contains 16 pixels, plus 4 prescan pixels. The prescan pixels are provided because of charge disturbance effects at the output gate when serial register clocking starts, affecting the measured pixel values for the first few pixels clocked out of the serial register. The prescan pixel values are normally discarded during the read out process. The 10 serial registers are clocked in parallel, and the corresponding video outputs are digitized in parallel, reducing by a factor of 10 the time required to digitize the pixel values from each row of the frame store.

A SciMeasure readout system is used with the CCID-66 and is also one of the readout options planned for the CCID-74. The SciMeasure readout system clock patterns for the imager, frame store, and serial register clocks, and the CCD reset and output gates, as well as the video output clamp and sample, the A to D conversion trigger, and a start of line and start of frame signal are all generated by data patterns stored in a random access memory (RAM). One bit from the pattern RAM corresponds to each signal, and the patterns are clocked out of the memory at a 50 MHz rate, making the minimum high or low period for each signal 20 ns.

Non-interleaved Read Out

The readout process for the CCID-74 in non-interleaved mode, where each row of pixels is transferred into the serial registers from the frame store after all of the pixels have been clocked out of the serial register, is shown in Figure 5.

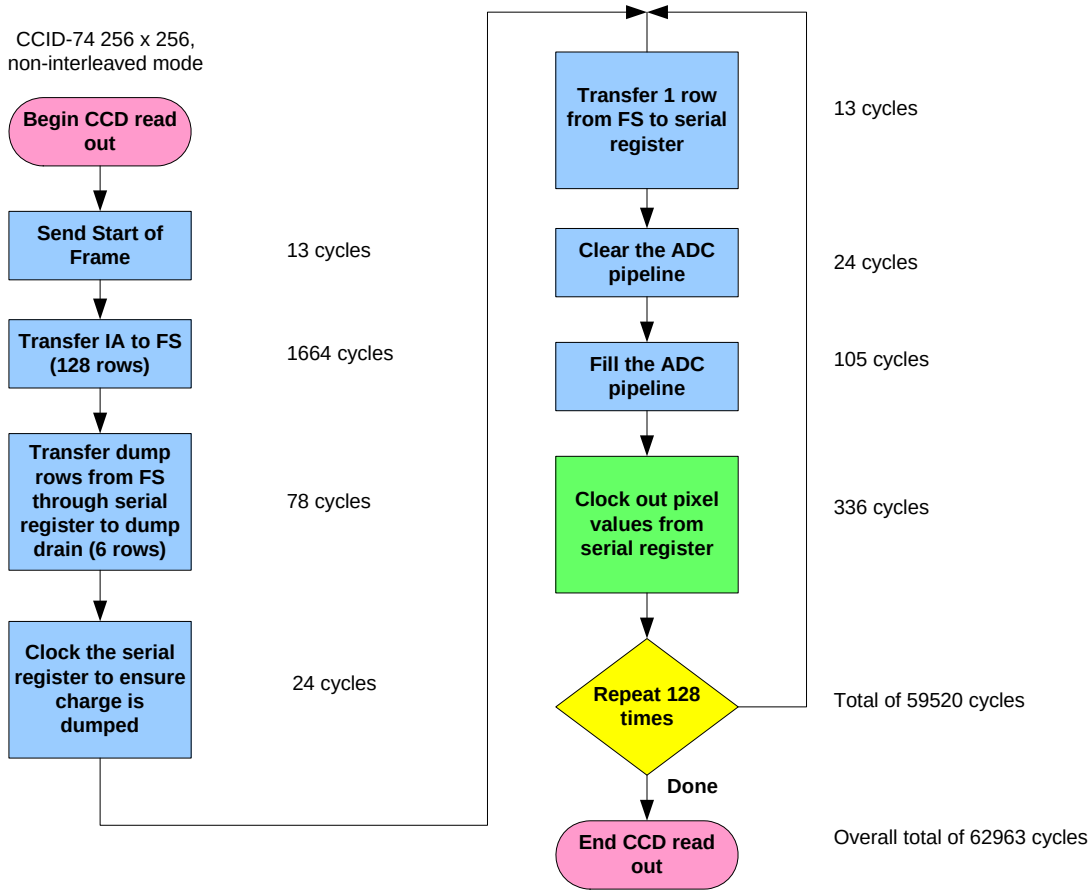

Figure 5: Non-interleaved CCID-74 readout, 2.38 MHz pixel clock frequency

The left hand side of Figure 5 shows the steps required to transfer the imager array to the frame store, and the right hand side shows the steps required to transfer each row from the frame store to the serial

registers and then clock out and digitize the pixels. The steps in Figure 5 correspond to the entries in Table 2 which describes the timing calculations for the non-interleaved readout.

Read out process	**Calculation**
Begin CCD read out	
Send start of frame	Tsof=13*clock_period
Transfer IA to FS	Tstorage_rows = (yrows/2)*trow
Transfer dump rows through serial register to dump drain	Tdump_rows = (2*dump_rows)*trow
Clock the serial register to ensure all charge is dumped	Tserial_clear = tpixel_period*((xpixels/(nVideo/2)+xprescan)
Transfer 1 row from FS to serial register	Timager_row = trow
Clear the ADC pipeline	Tpipeline_clear = xprescan*6*clock_period
Fill the ADC pipeline	Tpipeline_fill =5*tpixel_period
Clock out pixel values from the serial register	Tread_pixels = tpixel_period*(xpixels/(nVideo/2))
(Repeat 129 times)	Tread = (yrows/2)*(Timager_row+Tpipeline_clear+Tpipeline_fill+Tread_pixels)
End CCD read out	Tframe=Tsof+Tstorage_rows+Tdump_rows+Tserial_clear+Timager_rows +Tread+(13*clock_period)

Table 2: Non-interleaved readout timing calculations

The values of the constants clock_period, trow, tpixel_period, xprescan, dump_rows, xpixels, yrows, and nVideo are shown in Table 3 along with the results of the timing calculations assuming a certain number of controller clock cycles or periods per pixel, which also determines the pixel readout frequency (fpixel).

At the top of Table 3 we list the timing assumptions. We assume a row to row transfer time of 0.26 μs, and a pixel period of 0.42 μs, corresponding to a pixel read out frequency of 2.381 MHz. Below the timing assumptions we list the device format assumptions: the number of prescan pixels, and the number of extra rows provided on each half of the imager array to allow for light shield alignment as discussed earlier.

The device has 256 pixels in 256 rows, and can be read out through either 32 or 64 video outputs. As described previously every 16 columns of the device are provided with a serial register. This 16 pixel serial register can be read out through one or two video outputs. When two video outputs are used the effective length of the serial register is 8 pixels. Associated with each video output are 4 prescan pixels.

The resulting read out time calculations are summarized in the eleven rows under the heading "Timing" in Table 3. The total read out time, or time per image frame (T_{frame}) for the 32 video output mode is 1259.26 µs, corresponding to ~794 frames per second (fps) as shown in column 2 in the timing section. The corresponding number of controller clock cycles is shown in column 5 of the timing section.

Non-interleaved mode
CCID-74

Timing assumptions					
SciMeasure controller clock period	clock_period	0.020	0.020	0.020	µs
Row transfer time	trow	0.260	0.260	0.260	µs
Number of clock periods/pixel	clocks_pixel	21	21	13	
Pixel period	tpixel_period	0.420	0.420	0.260	µs
Pixel read out frequency	fpixel	2.381	2.381	3.846	MHz
Device format assumptions					
Serial register prescan pixels	xprescan	4	4	4	
Light shield alignment rows	dump_rows	3			

Device Size							
xpixels		256	256	256			
yrows		256	256	256			
nVideo		32	64	64			
Pixels per serial register		16	8	8			
Timing		µs	µs	µs	cycles	cycles	cycles
Tsof		0.26	0.26	0.26	13	13	13
Tstorage_rows		33.28	33.28	33.28	1664	1664	1664
Tdump_rows		1.560	1.560	1.560	78	78	78
Tserial_clear*		0.48	0.48	0.48	24	24	24
Timager_row		0.260	0.260	0.260	13	13	13
Tpipeline_clear		0.48	0.48	0.48	24	24	24
Tpipeline_fill		2.100	2.100	1.300	105	105	65
Tread_pixels		6.720	3.360	2.080	336	168	104
Tread		1223.680	793.600	527.360	61184	39680	26368
Tframe		1259.260	829.180	562.940	62963	41459	28147
Frame rate (fps)		794.12	1206.01	1776.39			

Read out time based on timing and device assumptions given above

Target frame rate (fps)	1000	1500	2000
Frame time (µs)	1000.000	666.667	500.000
Overhead (µs)	130.300	130.300	130.300
Tread (µs)	869.700	536.367	369.700
Tpixels (µs)	6.795	4.190	2.888
tpixel_period (µs)	0.324	0.322	0.222
Number of clock periods/pixel	16.177	16.117	11.109
fpixel (MHz)	3.091	3.102	4.501

Required read out timing for a given target frame rate

* = serial register is cleared by opening the dump drain and clocking it for 4 pixels at max. rate.

Table 3: CCID-74 timing calculations, non-interleaved mode

At the bottom of Table 3 we work the problem backwards from the frame rate to the required pixel read out frequency, and in this example if we want to achieve a frame rate of 1000 Hz, retaining the

assumption of a row to row transfer time of 0.26 μs, and the same device format assumptions, we would have to use a pixel read out frequency of 3.091 MHz.

The total read out time, or time per image frame (T_{frame}) for the 64 video output mode is 829.18 μs using a pixel clock frequency of 2.381 MHz, corresponding to ~1206 Hz as shown in column 3 in the timing section. The corresponding number of controller clock cycles is shown in column 6 of the timing section. Increasing the pixel clock frequency to ~3.85 MHz (the highest rate used with the CCID-66) results in a frame rate of ~1776 Hz for the 64 video output mode as shown in column 4 of the timing section.

As the bottom part of Table 3 indicates, achieving a frame rate of 2000 Hz would require a 4.5 MHz pixel clock rate. However, using the interleaved read out mode allows a significant reduction in the required pixel clock rates as discussed in the next section.

Interleaved Read Out

As described in the discussion on the CCID-66 performance earlier in this document, an interleaved readout mode has been demonstrated in which each row in transferred to the frame store as soon as the last pixel from the previous row enters the prescan pixel segment of the serial register. The readout process, shown in Figure 6, becomes a little more complex due to the need to establish the correct state in the serial register and the read out system ADC pipeline after transferring the first row from the frame store to the serial register, and then to interleave the row transfers with the serial register clocking process. The corresponding timing calculations are shown in Table 4.

The left most process steps in Figure 6 transfer the imager array to the frame store. The center column shows the process for the transfer of the first row to the serial register, and the process for the transfer of the next 126 rows, where each row transfer is simultaneous with one pixel of the readout. The right column shows the process for the transfer of the last row, and again the row transfer is simultaneous with one pixel of the readout.

As was done in Table 3, at the top of Table 5 we list the timing assumptions. We assume a row to row transfer time of 0.26 μs, and a pixel period of either 0.42 μs or 0.38 μs, corresponding to a pixel read out frequency of 2.381 or 2.632 MHz. Below the timing assumptions we list the device format assumptions: the number of prescan pixels, and the number of extra rows provided on each half of the imager array to allow for light shield alignment as discussed earlier.

The resulting read out time calculations are shown in Table 5 in the 26 rows under the heading "Timing". The total read out time, or time per image frame (T_{frame}) for the 32 video output mode is 952.18 μs, corresponding to ~1050 frames per second (fps) as shown in column 2 in the timing section. The corresponding number of controller clock cycles is shown in column 5 of the timing section.

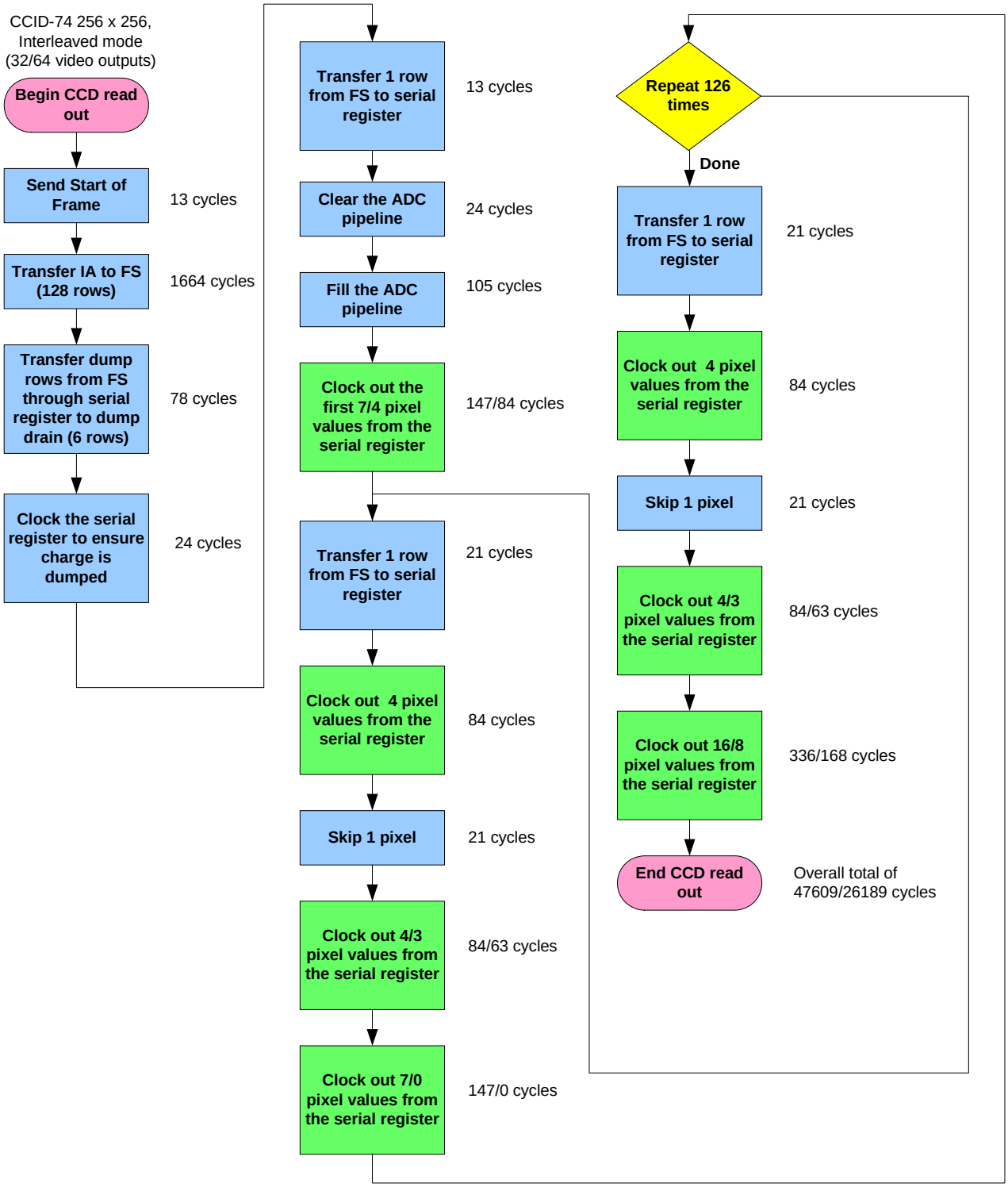

Figure 6: Interleaved CCID-74 readout, 2.38 MHz pixel clock frequency, 32 and 64 video output modes

Begin CCD read out	
Send start of frame	Tsof=13*clock_period
Transfer IA to FS	Tstorage_rows = (yrows/2)*trow
Transfer dump rows through serial register to dump drain	Tdump_rows = (2*dump_rows)*trow
Clock the serial register to ensure all charge is dumped	Tserial_clear = tpixel_period*((xpixels/(nVideo/2))+xprescan)
First row	
Transfer 1 row from FS to serial register	Timager_row = trow
Clear the ADC pipeline	Tpipeline_clear = xprescan*6*clock_period
Fill the ADC pipeline	Tpipeline_fill =5*tpixel_period
Clock out 7 or 4 pixel values from the serial register	Tread_pixels7/4 = tpixel_period*7(or *4)
Middle rows (repeated 126 times)	
Transfer 1 row from FS to serial register and read pixel	Tinterleave_row = tpixel_period
Clock out 4 pixel values from the serial register	Tread_pixels4 = tpixel_period*4
Skip 1 pixel	Tskip_pixel = tpixel_period
Clock out 4 or 3 pixel values from the serial register	Tread_pixels4/3 = tpixel_period*4 (or *3)
Clock out 7 or 0 pixel values from the serial register	Tread_pixels7/0 = tpixel_period*7(or *0)
Last row	
Transfer 1 row from FS to serial register and read pixel	Tinterleave_row = tpixel_period
Clock out 4 pixel values from the serial register	Tread_pixels4 = tpixel_period*4
Skip 1 pixel	Tskip_pixel = tpixel_period
Clock out 4 or 3 pixel values from the serial register	Tread_pixels4/3 = tpixel_period*4 (or *3)
Clock out 16 or 8 pixel values from the serial register	Tread_pixels16/8 = tpixel_period*16(or *8)
	Tread = Tread_first_line+Tread_middle_lines+Tread_last_line
End CCD read out	Tframe=Tsof+Tstorage_rows+Tdump_rows+Tserial_clear_Timager_rows +Tread+(13*clock_period)

Table 4: Interleaved readout timing calculations

Interleaved mode
CCID-74
Timing assumptions

SciMeasure controller clock period	clock_period	0.020	0.020	0.020	µs
Row transfer time	trow	0.260	0.260	0.260	µs
Number of clock periods/pixel	clocks_pixel	21	21	19	
Pixel period	tpixel_period	0.420	0.420	0.380	µs
Pixel read out frequency	fpixel	2.381	2.381	2.632	MHz

Device format assumptions

Serial register prescan pixels	xprescan	4	4	4
Light shield alignment rows	dump_rows	3		

Device Size

xpixels	256	256	256
yrows	256	256	256
nVideo	32	64	64
Pixels per serial register	16	8	8

Read out time based on timing and device assumptions given above

Timing	µs	µs	µs	cycles	cycles	cycles
Tsof	0.26	0.26	0.26	13	13	13
Tstorage_rows	33.28	33.28	33.28	1664	1664	1664
Tdump_rows	1.560	1.560	1.560	78	78	78
Tserial_clear*	0.48	0.48	0.48	24	24	24
Timager_row	0.260	0.260	0.260	13	13	13
Tpipeline_clear	0.48	0.48	0.48	24	24	24
Tpipeline_fill	2.100	2.100	1.900	105	105	95
Tread_pixels7/4	2.940	1.680	1.520	147	84	76
Tread_first_line	**5.780**	**4.520**	**4.160**	289	226	208
Tinterleave_row	0.420	0.420	0.380	21	21	19
Tread_pixels4	1.680	1.680	1.520	84	84	76
Tskip_pixel	0.420	0.420	0.380	21	21	19
Tread_pixels4/3	1.680	1.260	1.140	84	63	57
Tread_pixels7/0	2.940	0.000	0.000	147	0	0
Tread_middle_lines	**899.640**	**476.280**	**430.920**	44982	23814	21546
Tinterleave_row	0.420	0.420	0.380	21	21	19
Tread_pixels4	1.680	1.680	1.520	84	84	76
Tskip_pixel	0.420	0.420	0.380	21	21	19
Tread_pixels4/3	1.680	1.260	1.140	84	63	57
Tread_pixels16/8	6.720	3.360	3.040	336	168	152
Tread_last_line	**10.920**	**7.140**	**6.460**	546	357	323
Tread	916.340	487.940	441.540	45817	24397	22077
Tframe	952.180	523.780	477.380	47609	26189	23869
Frame rate (fps)	1050.22	1909.20	2094.77			

Target frame rate (fps)	1000	1500	2000
Frame time (µs)	1000.000	666.667	500.000
Overhead (µs)	35.840	35.840	35.840
Tread (µs)	964.160	630.827	464.160
Tpixels (µs)	7.533	4.928	3.626
tpixel_period (µs)	0.443	0.548	0.403
Number of clock periods/pixel	22.154	27.380	20.146
fpixel (MHz)	2.257	1.826	2.482

Required read out timing for a given target frame rate

* = serial register is cleared by opening the dump drain and clocking it for 4 pixels at max. rate.

Table 5: CCID-74 timing calculations, interleaved mode with 32 or 64 video outputs

At the bottom of Table 5 we work the problem backwards from the frame rate to the required pixel read out frequency, and in this example if we want to achieve a frame rate of 1000 Hz, we now require a pixel read out frequency of ~2.26 MHz, compared to 3.091 MHz in non-interleaved mode.

The total read out time, or time per image frame (T_{frame}) for the 64 video output mode is 523.78 μs using a pixel clock frequency of 2.381 MHz, corresponding to ~1909 frames per second (fps) as shown in column 3 in the timing section. The corresponding number of clock cycles is shown in column 6 of the timing section. Increasing the pixel clock frequency to ~2.48 MHz results in a frame rate of ~2000 Hz for the 64 video output mode as shown in column 4 of the timing section. Because the number of controller clock periods is constrained to be an integer in practice, if 20 clock periods per pixel are used the actual frame rate is ~1997 Hz, and with 19 clock periods per pixel the actual frame rate is ~2094 Hz.

Timing Considerations

It is important to keep in mind that the row to row transfer time, and the pixel read out frequency cannot be established arbitrarily. The minimum value for the row to row transfer time is limited by the duration and overlap of each of the three row clock phases. This is determined experimentally, with the row clock timing set as required to ensure that the parallel (row to row transfer) charge transfer efficiency (CTE) requirement is met. Similarly the pixel read out frequency is limited by the duration and overlap of each of the three serial register clock phases. This is also determined experimentally, with the serial register clock timing set as required to ensure that the serial (pixel to pixel transfer) charge transfer efficiency (CTE) requirement is met.

The pixel read out frequency is also limited by at least two other factors, the acceptable level of read noise, and the settling time of the output amplifier and the signal chain from the output amplifier to the read out system analog to digital converter (ADC). The former may be determined by performing photon transfer measurements and generating a curve that allows diagnosis of the actual read noise under a given set of operating conditions. For a given pixel read out frequency the input filters on each channel of the read out system must be adjusted to match the required input bandwidth. As the rate at which pixels are read out is increased, the upper frequency cut-off of the read out system input filters must increase, resulting in increased read noise per pixel.

The required settling time for the output amplifier and the read out system signal chain are also be determined experimentally, either using instrumentation or photon transfer measurements at various pixel read out frequencies.

PERFORMANCE PREDICTIONS

The performance predictions for the CCID-74 are based on measurements of the CCID-66 devices. The SciMeasure read out system built for the CCID-56b/d and CCID-66 has demonstrated a very low instrumental noise floor, and based on experience to date we do not expect any deterioration of that low noise performance when systems are configured with larger numbers of video outputs.

Read Noise

The system level (detector and read out system) read noise estimates for the CCID-74 are based on test results for the CCID-66. In Figure 7 a physics based theoretical curve for read noise as a function of pixel read out frequency is shown for a read noise voltage corresponding to 40 nV/√Hz for the detector and read out system combined, and assuming a responsivity of 25 μV/e- for the planar JFET first amplifier stage. This corresponds to read noise of 1.6 electrons at a 1 MHz pixel read out frequency. The results of actual testing (Table 1) for the CCID-66 are also shown

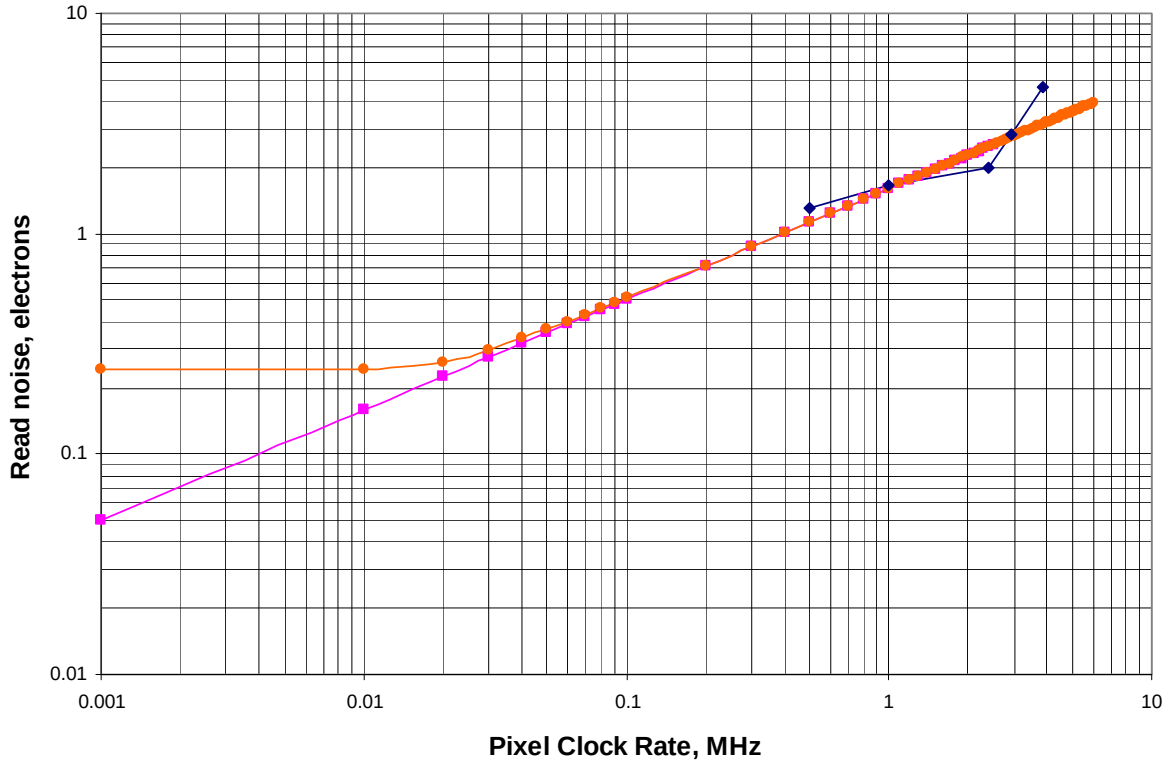

Figure 7: CCID-66 Read noise vs. pixel read out frequency (blue curve) and physics based theoretical curves (orange with 1/f noise, pink without) assuming a detector responsivity of 25 μV/e- and a detector + read out system noise voltage of 40 nV/√Hz.

Dark Current

In low noise applications it is normally desirable to ensure that the detector is operating under read noise limited conditions. For high frame rate applications the impact of dark current is reduced due to the short duration of each frame time, but the operating temperature remains the key consideration in reducing dark current to the level required to ensure read noise limited operation. It should be noted that process improvements, like those used on the most recent CCID-56b devices have significantly reduced the dark current figure of merit, further reducing the cooling requirements.

In Figure 8 the effect of dark current on SNR as a function of temperature is shown for various frame rates, assuming a median value (1 nA/cm^2) for the dark current figure of merit (see appendix A). SNR here is normalized to 1, where 1 represents operation where dark current does not contribute to the image noise. As the figure indicates, temperatures between -20 and -30 ºC, commonly achievable with thermo-electric coolers (TECs) will provide read noise limited operation down to at least 500 fps.

For operation at lower frame rates, additional cooling is required. In the case of the CCID-56b, operation as a natural guide star wavefront sensor in an adaptive optics system can require frame rates as low as 55 fps, and for this reason a custom vacuum cryostat cooled with a Cryotiger auto-cascade closed cycle refrigerator was developed for the CCID-56. For higher frame rate applications a TEC should provide sufficient reduction of dark current.

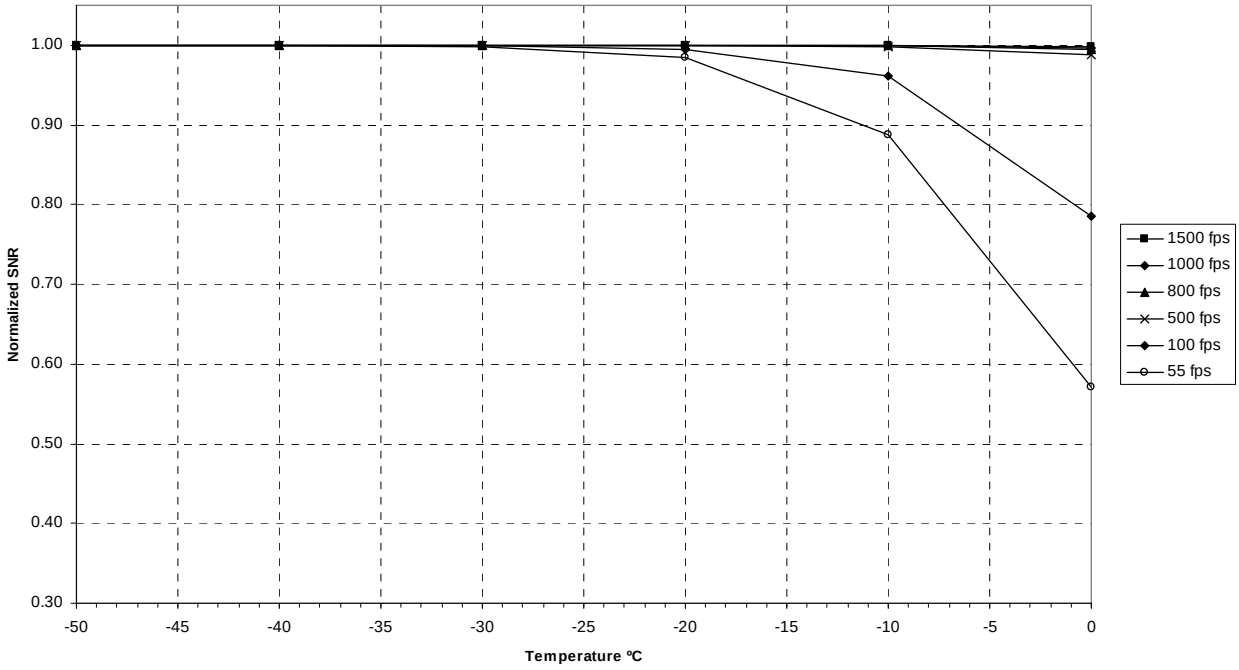

Figure 8: Normalized SNR versus temperature at various frame rates

Quantum Efficiency

Quantum efficiency (QE) for a thinned back illuminated CCD is determined by three major factors, the technique used to eliminate the backside potential well that forms after thinning of the CCD substrate, the final thickness of the CCD substrate, and the AR coating applied to the CCD backside.

MIT/LL now uses a molecular beam epitaxy (MBE) process for backside treatment. In addition to improving the dark current this process results in a very thin accumulation layer on the backside of the CCD, improving the QE.

The thickness of the CCD is a key variable in determining the longest wavelength at which the maximum QE can be obtained. This is because the distance that a photon travels through the light

sensitive silicon backside layer is a function of wavelength, referred to as the absorption depth. For example, the absorption depth in silicon at 700 nm is 8.5 µm, while at 900 nm the absorption depth is 62 µm. The long wavelength limit for a CCD is ultimately set by the wavelength at which silicon effectively becomes transparent to the incident light, ~1100 nm.

As mentioned earlier a version of the CCID-56, designated the CCID-56d has been produced using the corners of Pan-STARRS orthogonal transfer array (OTA) wafers with a 45 µm substrate thickness. QE measurements for the Pan-STARRS OTA devices with a 45 µm show QE that is essentially identical to the MIT/LL CCID-20 red enhanced devices (used in the WMKO HIRES upgrade among other instruments). A 75 µm substrate thickness has also been used for OTA devices and this offers an increase of 10 to 50% in QE over the wavelength range from 800 to 1000 nm.

To date AR coatings have been deposited using thermal evaporation in order to avoid damage to the CCDs, but evaporation limits the selection of materials that can be used. As a result MIT/LL has explored alternative techniques for applying the AR coating to the CCD. By using ion assisted deposition (IAD) the quality of the AR coating is improved. Most recently an IAD coating with very good mid-band performance has been developed called "Bodacious Black". A quantum efficiency curve for this coating on a larger detector (a CCID-20) with a 36 µm substrate thickness is shown in Figure 9 along with a curve for the CCID-56d from measurements made in August 2007, and a curve for a 75 µm substrate thickness orthogonal transfer array (OTA) from measurements made by the Pan-STARRS project in mid-2007

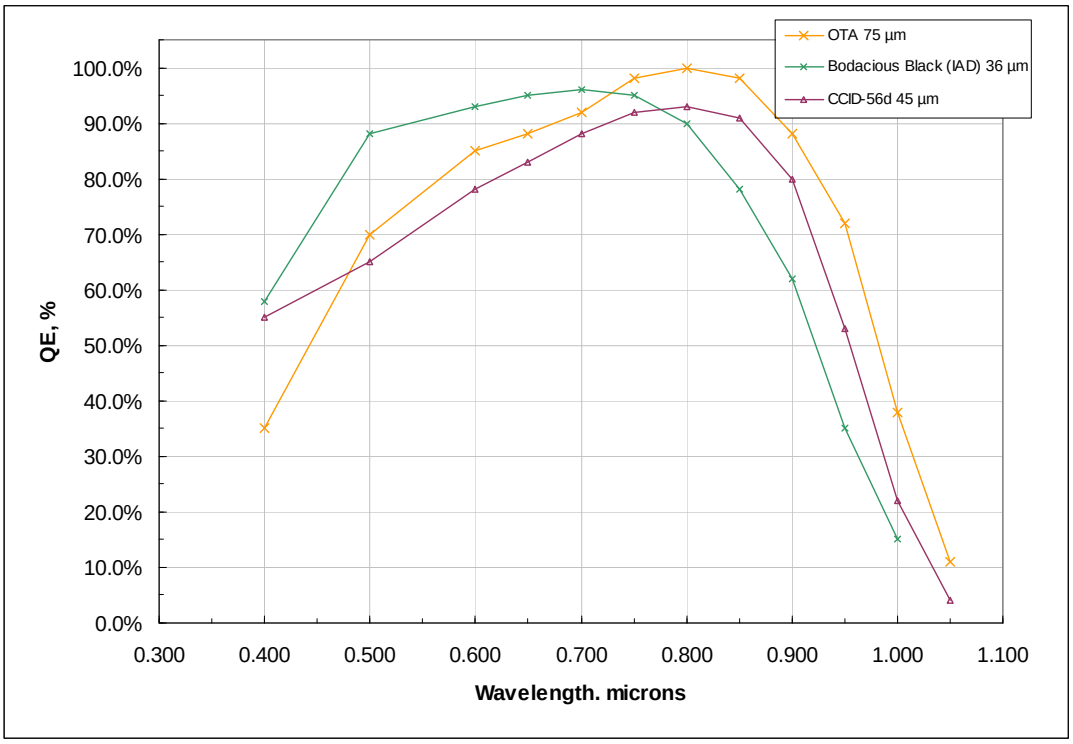

Figure 9: CCID-56, Pan-STARRS OTA, and Bodacious Black QE curves

The CCID-56b devices have been specified with an AR coating that yields a QE peak around 0.7 μm. This was selected as a compromise between optimizing NGS performance and optimizing performance for sodium laser guide star wavefront sensing. For strictly NGS operation QE may be optimized further into the red end of the spectrum. The CCID-74 could be produced with either the 45 μm or 75 μm (or thicker) substrates, with the thicker substrate allowing an extended red response.

It should be kept in mind that at wavelengths of 0.9 μm and longer the relatively thin substrates will cause fringing due to interference effects in the substrate. However, the fringe amplitudes will typically be less than 2% of the peak and for a wavefront sensing application this level of fringing is not expected to present a significant problem.

SPECIFICATIONS

The final specifications of the CCID-74 device are summarized in the following sections.

Features

- Split frame transfer with a light shield over the frame store and serial registers
- 3 additional rows provided in the imager and each half of the frame store to accommodate light shield alignment
- 64 video outputs (32 for each half of the frame store)
- 16 serial registers for each half of the frame store with a multiplexer at pixel 8 in the serial register to support 32 or 64 channel read out
- Low noise, two stage planar JFET output structure on each video output
- Dual output gate for each video output
- Summing well at the end of each serial register
- Dump drain parallel to the serial register
- A single bias input for all 32 output amplifiers on each half of the frame store

Packaging

- Devices are wafer probed prior to packaging for functionality and cosmetic quality
- 131 pin hermetic package with broad band AR coated window and 2 stage TEC
- U309 buffer provided for each output port
- Bypass capacitors on VDD, RDD and output gate
- A thermistor next to the CCD chip on the hermetic package ceramic interposer, both leads pinned out

Goal Parameters

Parameter	*Goal*	*Min.*	*Typ.*	*Max.*	*Units*	*Notes*
Pixel size	21	18	-	24	µm	1
Responsivity	≥ 40	25	TBS	-	µV/ e^-	2,3
Responsivity non-uniformity	< 10	-	TBS	TBS	%, p-p	3
Read noise at 3.58 MHz	< 3	-	< 3.5	< 5	e^- rms	4
Read noise at 2.38 MHz	< 2	-	< 2.5	< 3	e^- rms	4
Read noise at 1 MHz	< 1.2	-	< 1.7	< 2	e^- rms	4
Dark current	< 50	-	TBS	< 100	e^-/pixel/sec	3,5
Serial clock rate	5 x 10^6	-	-	TBS	Hz	
Crosstalk	10,000:1	5,000:1	-	-	n/a	6

Notes:
1. Square pixels
2. Test results from the CCID-56d show a responsivity of 25 µV/ e^-.
3. TBS: to be specified.
4. Read out rate per port, no binning.
5. 21 µm pixels, device temperature of -30 ºC.
6. Between any 2 amplifiers.

Typical Parameters

Parameter	*Min.*	*Typ.*	*Max.*	*Units*	*Notes*
Substrate thickness	75	-	-	μm	
QE @ 400 nm	55	58	-	%	1
QE @ 500 nm	65	88	-	%	1
QE @ 600 nm	75	93	-	%	1
QE @ 700 nm	85	96	-	%	1
QE @ 800 nm	90	93	-	%	1
QE @ 900 nm	80	80	-	%	1
QE @ 950 nm	50	53	-	%	1
QE @ 1000 nm	20	22	-	%	1
QE non-uniformity	-	< 5	< 8	%, p-p	2
Σ	-	4	<8	μm	3
CTE	0.99995	0.99999	-	:1	4
Pixel Full Well Capacity	25,000	50,000	-	e^-	
Summing Well Capacity	25,000	50,000	-	e^-	5
Serial Register Capacity	25,000	50,000	-	e^-	5
Non-linearity	-	<1	TBS	%	6,7
Vertical transfer rate	2.5	-	4	MHz	
Operating temperature	-120	-30	30	ºC	8
Output window flatness	1/10	-	-	λ	9
Window tip/tilt	-	-	TBS	°	10

Notes:
1. Mean value over all active imager pixels, measured with a 10 nm line width source. Bodacious Black IAD coating on 75 μm thick substrate.
2. % non-uniformity with respect to the mean QE at all wavelengths where fringing does not occur.
3. PSF including effects of charge diffusion.
4. Serial and parallel, measured at a 3.85 MHz vertical transfer rate and a 3.58 MHz per port read out rate.
5. In all cases the summing well and serial register capacities are not less than the pixel capacity.
6. Incident flux to output transfer function non-linearity over the full range from dark to saturation.
7. TBS: to be specified.
8. Minimum operating temperature corresponds to the lowest temperature where CTE and other device parameters remain within specifications. Actual operating temperature depends on the desired dark current. Devices are capable of room temperature operation but the dark current rate may be excessive.
9. 1/10 of a wavelength of light at 632.8 nm.
10. Tip/tilt of output window plane with respect to the detector image plane.

Cosmetics

All defects are characterized at a temperature of -30 °C unless noted otherwise.

Parameter	*Min.*	*Goal*	*Max.*	*Units*	*Notes*
Bad Columns	-	0	0	per CCD device	1
Hot Pixels	-	0	2	per CCD device	2
Dark Pixels	-	< 3	4	per CCD device	3
Traps	-	0	0	per CCD device	4

Notes:
1. A bad column is one that contains at least 10 hot or dark pixels.
2. A pixel is considered hot when the spontaneous electron generation rate is greater than 100 times the modal dark current.
3. A pixel is considered dark when the responsivity of that pixel with a flux intensity that produces approximately 50% full well over the wavelength range of 0.3μm to 1.1μm is below the local mean value by more than 2 times the local QE non-uniformity. Local is defined as a region of 8 x 8 pixels.
4. Pixels where >10 e^- of charge is held temporarily.

APPENDIX A: DARK CURRENT ESTIMATION

Janesick (2000) gives an equation for determining CCD dark current based on temperature, a "dark current figure of merit" or D_{FM} and the pixel area. D_{FM} must be determined from material properties and then refined experimentally. The equation for dark current is as follows:

$$D_R(e^-) = 2.5x10^{-15} P_s D_{FM} T^{1.5} e^{-E_g/2kT} \quad (1)$$

where :

D_R is the dark current in e^-/pixel/s

P_s is the pixel area in cm^2

D_{FM} is the dark current figure of merit in nA/cm^2

T is the temperature in Kelvin

E_g is the bandgap energy in electron volts

k is Boltzman's constant

Dark current figures of merit for MIT/LL CCDs normally range from 2 to 4 nA/cm^2, but recent improvements using an MBE process have reduced the range by a factor of ~ 4. Figure 10 shows the dark current versus temperature curves that result from D_{FM} values ranging from 0.5 to 1.5 nA/cm^2 with 21 μm square pixels.

As Figure 10 illustrates, the rate at which dark current is generated per unit time is a function of temperature. Higher frame rates reduce the dark current noise that accumulates in each pixel, and for a given frame rate the noise contributed by dark current can be effectively eliminated by cooling the device. Since cooling costs money, and where a TEC is used, it also increases power dissipation in the vicinity of the detector, the device temperature should not be set lower than that required to ensure read noise limited operation, defined as the operating regime where image SNR depends on photon noise and read noise, and not dark current.

For a given set of operating assumptions the SNR may be computed using equation 2.

$$SNR = \frac{n_p}{\sqrt{n_p + P_a(D_R^2 + R_N^2)}} \quad (2)$$

where :

n_p is the number of detected photons per subaperture

P_a is the number of pixels per subaperture

D_R is the dark current, e^-/pixel/s

R_N is the read noise, e^-

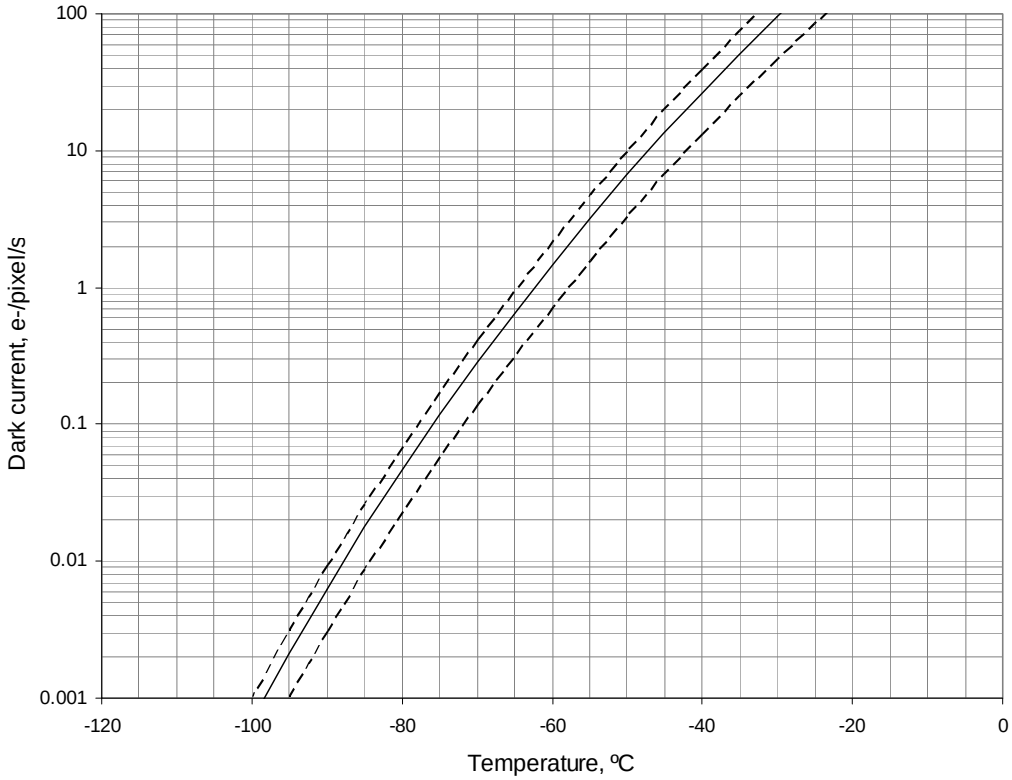

Figure 10: Dark current vs. temperature for D_{FM} = 0.5, 1 and 1.5 nA/cm^2

APPENDIX B: READ NOISE

The results of read noise tests on both front and back illuminated versions of the CCID-56b and CCID-66 are available to anchor the read noise performance of the planar JFET output amplifier. The measurements made using front illuminated devices were hindered by excessive dark current due to incomplete removal of the backside n+ layer used to absorb contaminants during the wafer fabrication process.

The front illuminated devices were evaluated at room temperature (~ 20 ºC) where the dark current was high enough that read noise measurements using over scan (continuing to read the serial register after the last image pixel is clocked out) or photon transfer were unusable. The corresponding D_{FM} for these devices was estimated at 1800 nA/cm^2. Responsivity was determined using photon transfer to be between 0.14 and 0.19 e^-/DN including the gain setting of the read out system.

An alternative method was then used to evaluate the read noise in which the summing well was held in summing mode during the read out, effectively blocking the output of the serial register. The resulting noise contribution is then expected to be due only to the device output amplifier, the output buffer in the device package, the interconnections and the detector controller and power supplies. With this method the noise measured at a 1 MHz pixel read out frequency was between 0.98 e^- and 1.33 e^-, assuming responsivities of 0.14 and 0.19 e^-/DN respectively. Additional testing at a read out frequency of 1.5 MHz resulted in read noise of ~1.5 e^- (using the responsivity of 0.14 e^-/DN). These measurements were performed by SciMeasure using a 20 channel Little Joe read out system developed for the CCID-56b.

The back illuminated devices packaged by MIT/LL have shown exceptionally low dark current, corresponding to a D_{FM} of 0.5 nA/cm^2, about 4 times lower that the best dark current that is typical of MIT/LL devices. Measurements made by SciMeasure for a back illuminated CCID-56b has shown read noise of ~1.8 e^- at a 1 MHz pixel read out frequency, but based on photon transfer curves these devices seem to have a lower responsivity, approximately one half that of the front illuminated devices, or ~20 μV/e^-. This is not consistent with the responsivity of > 40 μV/e^- measured by MIT/LL for the same device using a Fe-55 source. If 40 μV/e^- is the actual responsivity then the correct read noise value is a factor of two lower.

Measurements made by MIT/LL using their test system have consistently shown higher read noise levels that those obtained using the SciMeasure read system. This is attributed to the better shielding and integration of the SciMeasure system as well as their overall design quality. For similar back illuminated devices MIT/LL obtained ~2.5 e^- at a 1 MHz pixel read out frequency and 1.1 e^- at a 70 KHz pixel read out frequency. The slope of this curve deviates from the expected shape, suggesting that there may be a higher noise floor in the read out system or test configuration at MIT/LL.

Based on the measurements made with the CCID-66, if we assume a 25 μV/e^- responsivity, and read noise at 1 MHz between 1 and 2 electrons, the noise voltage for the detector and read out system combined is between 30 and 50 nV/√Hz.

From this we can derive a curve for read noise as a function of pixel read out frequency as shown in Figure 7. Here we assume that for CDS sampling the white noise limited component is described by:

$$Eout = Enoise * \sqrt{f_1 - f_2} \tag{3}$$

Where :

$$f_1 = \frac{1}{2} f_{pixel}$$

$$f_2 = \frac{3}{2} f_{pixel}$$

and

$Enoise$ is the readout system noise voltage in $nV/\sqrt{Hz}$

Eout is converted to electrons of read noise using the assumed responsivity of 25 μV/e$^-$.

We also assume that the system noise floor is much lower than the signal, that is, about 1 μV, and compute the 1/f noise component (*Ef*) as follows (Janesick 2000):

$$Ef = \sqrt{Efloor^2 * (1 + \frac{f_c}{f_{pixel}})} \tag{4}$$

Where :

f_c is the $\frac{1}{f}$ corner frequency

REFERENCES

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