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| Caltech |
| Controller Testing for ZTF |
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**Preliminary STA Controller Testing Results**

1.0, September 14, 2015

Caltech

# Introduction

Focal plane CCDs at Palomar are ubiquitous and need support electronics for biasing and image acquisition. It is advantageous to have the support electronics close to the CCD, and so the packaging of the controller electronics is an important aspect of the system. The performance of the astronomical instrument is directly related to the performance of the controller electronics. In this note, we describe the electrical specifications for the controller and the test procedures to confirm the electrical performance. This requirements and testing document applies to the single board controller unit which is the present anticipated design.

This document contains the preliminary results from testing the STA controller. This testing includes the ADC module noise, the clock card noise, and the DNL measurement for the ADC channel. Future tests will check the stability of the system by sending data from the controller to the host overnight.

# Testing method and equipment

The testing for the controller will consist of many loopback configurations and external signal input configurations. The loopback and input connections will occur on the test point connector on the transition card. This test point connector allows access to every signal which is used for connection to the CCDs in the mosaic.

The pins which are plugged into the test connector will have to change depending on the test desired. A list of the configurations is as follows:

1. Grounded ADC Input (ADC Module noise test)
   1. All ADC channels tested at once
2. Grounded ADC Input and Three Loopbacks (ADC Crosstalk module)
3. Function generator input to ADC Module and DIO output to function generator trigger(INL/DNL Test)
   1. All ADC channels tested at once
4. Clock distribution into the ADC Module (clock noise test, clock range test)
   1. 16 clocks tested at once (total of 18 per controller)
   2. Attenuator switched in/out for high clock levels
5. Bias distribution into the ADC Module (bias noise test)
   1. 16 biases tested at once (total of 30 per controller)
   2. Attenuator switched in/out for high bias levels
      1. Biases don’t change, how do we measure a level?

For the clock and bias testing, the test connector will need to be adjusted 2 times for the clock tests and 2 times for the bias tests.

## Software/computer configuration

These first requirements should be set in for all controllers, and are listed for completeness. (1) The environment variable PYTHONPATH is /home/ztf/devel/python. (2) ~/bin/archon\_tests is symbolically linked to PYTHONPATH/PHM/tests.py and is executable.

Run "git pull" in the ~/Software and ~/devel directories prior to attempting any tests.

Either vicd or goarchon -p 50060 must be running to communicate with the Archon controller.

# ADC Module Nosie

The signal chain and ADC Module will be used to make measurements for other parts of the system, therefore; the grounded input noise of the ADC Module will be necessary for many of the remaining controller tests. So it is necessary to have a good measurement of the ADC signal chain itself. To measure the noise in the ADC Module, the inputs to the signal chain are grounded. This requires the grounded input module which is plugged in to the transition card test point connector.

## Test Setup

Each ADC module has 4 channels, and all channels can be tested simultaneously. To measure the noise on each channel, data is taken in raw mode and analyzed for the standard deviation of the signal. For this test, the positive and negative inputs for the ADC channel are grounded and clamped by the magic board and the ACF file.

## Software Inputs

To run the test on all channels:

[ztf@ztf-cameraN YYYYMMDD]$ archon\_tests 'clamped\_noise()'

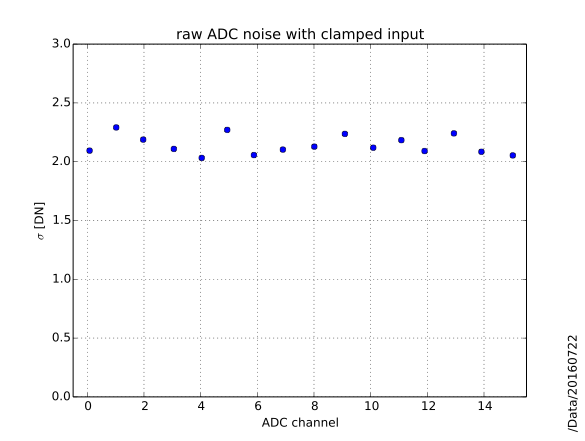
Move the files to their own directory (eg, ../YYYYMMDD\_ADC\_noise) then run the analysis script on all files (python):

>>> import PHM.noise as nn

>>> nn.plot\_clampednoiseVSchan(savefig=True)

## Data Products

A raw file will be produced for each channel on an ADC Module. Each one of these files will be analyzed simply as the standard deviation of the signal within the image. [The image will be stored and used as a basis for subtraction from other raw files for other controller tests. (NO, we will take reference data as needed in other tests)]



The figure above DOES have error bars, but they are smaller than the plot symbols.

# ADC DNL Test

The differential nonlinearity (DNL) is a measure of the difference between an actual step width and the ideal value of 1 LSB. This is the deviation from the ideal range of voltage mapped to 1 LSB. Larger step widths will favor certain codes over other codes and will adversely affect the digital representation of the analog signal. A DNL greater than 0.5 LSB means there will be missing codes in the converter which will never appear in the data stream. The DNL can be measured using a histogram test and sweeping the full voltage range of the converter.

## Test Setup

The Tektronix AFG3000 series function generator is the input to the ADC Module. The function generator is set to the following parameters:

Function: Triangle Wave

Frequency: 100 kHz

Voltage: 4.7 Vp-p

Offset: 0 mV

Phase: 0 degrees

Symmetry 50 %

Noise: 30 %

Mode: Burst with positive trigger

Trigger Delay: 0 ns

The INL/DNL test module routes the function generator signal to the input of all 4 channels on an ADC Module. In addition, the module routes DIO 1 from the LVDS board back to the trigger input of the function generator.

The trigger to the function generator ensures that the phase of each burst is the same so that the average voltage of the AC signal is 0 V. This keeps the signal centered within the ADC voltage range. The triggered burst mode makes the conversion synchronous with the function waveform and the same point on the input signal is sampled each period. The conversion noise is small enough so that all codes are not evenly converted, so noise was added to the signal for all codes to be sampled.

## Software Inputs

To run the test on all channels:

[ztf@ztf-cameraN YYYYMMDD]$ archon\_tests 'dnlinl()'

Move the files to their own directory (eg, ../YYYYMMDD\_dnlinl) then run the analysis script on all files (python):

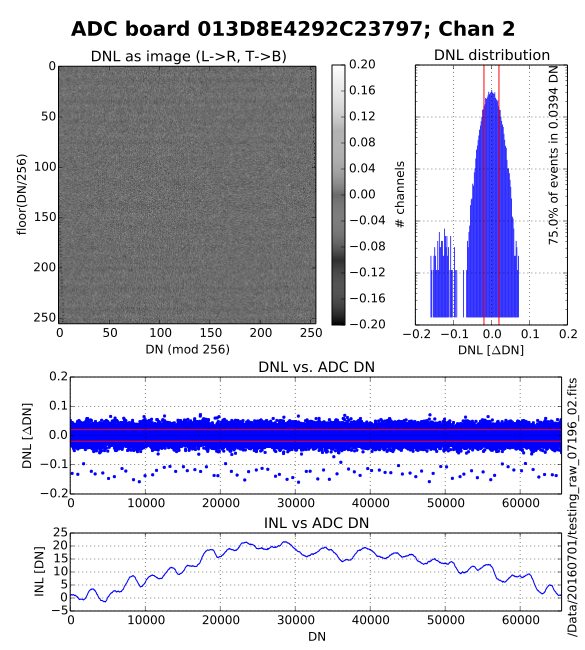
>>> import PHM.dnlinl as dd

>>> for jj in range(16):

>>> dd.measurement(jj).makefig(savefig=True)

Save the figures and delete the raw data files (they are HUGE!).

## Data Products



# ADC Module Crosstalk Test

In a multi-channel system, it is possible for one channel to share its signal with the neighboring channel. This effect can cause noise which is extremely difficult to subtract out of the image and is as variable as the images. Each ADC Module contains four signal chains, and it is within each ADC Module where the problem can be most severe. The crosstalk test will measure the signal on all fifteen grounded input channels while one channel receives a constant amplitude 1 MHz square wave.

Requirement?

## Test Setup

For this test, the crosstalk module will be used. This module will ground three inputs on the ADC Module while the remaining input receives a clock signal from a driver board. A constant loopback pattern will be fed into this channel while the raw signal at the grounded inputs are acquired. The samples which are taken during each cycle of the loopback pattern are co-added to make the measurement more sensitive to the crosstalk signal. A matrix can be made which will show the crosstalk in a channel versus the other three channels on the ADC Module. A matrix will be made for each ADC Module.

## Software Inputs

To run the test on all channels:

[ztf@ztf-cameraN YYYYMMDD]$ archon\_tests 'xtalk()'

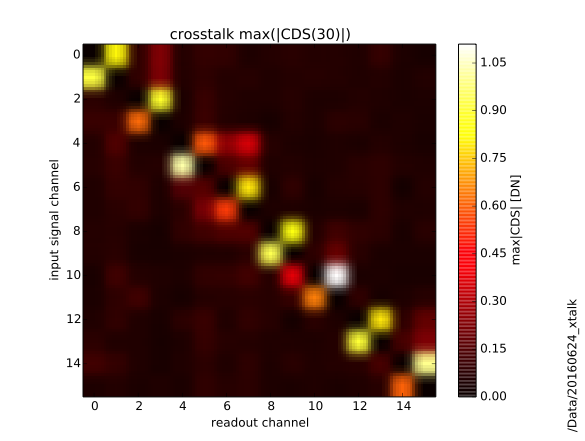
Move the files to their own directory (eg, ../YYYYMMDD\_xtalk) then run the analysis script on all files (python):

>>> import PHM.xtalk as x

>>> x.reduce(savefig=True)

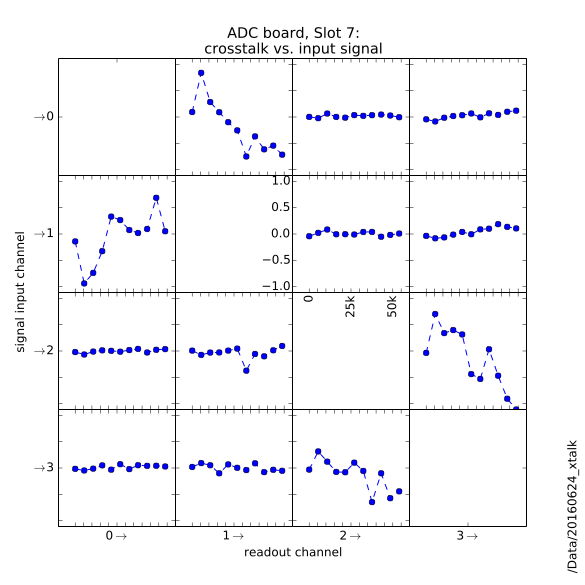
## Data Products

The controllers do not exhibit significant crosstalk. Thus, the summary output figure only shows the absolute value of the maximum CDS crosstalk measured with a 30 sample window.



(the original figure is not smeared out the way this is).

Since most of the "interaction" takes place within a board, we produce a more detailed summary figure for each board, indicating the measured CDS signal as a function of input amplitude.



# Clock Driver Noise

The signal chain and ADC Module will be used to measure the noise on the clock voltages. Therefore, this test requires the driver module and the ADC Module. For each voltage level, plot a histogram of the data and report the standard deviation of the resultant Gaussian (rms noise). The baseline noise of the ADC must be subtracted to arrive at the measurement of the clock rail noise and is given by:

Where emeasurement is the measured noise made in the above test setup, ebaseline is the baseline noise measured while the video processor input is grounded, and erail is the clock rail noise.

Measurement is only performed at +13V, which gives maximal noise.

## Test Setup

Use the magic board.

## Software Inputs

To run the test on all channels:

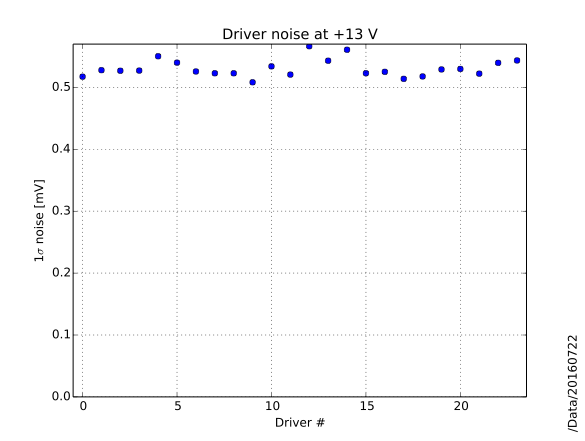
[ztf@ztf-cameraN YYYYMMDD]$ archon\_tests 'driver\_noise()'

Move the files to their own directory (eg, ../YYYYMMDD\_driver\_noise) then run the analysis script on all files (python):

>>> import PHM.driver as dd

>>> dd.plot\_noise(savefig=True)

## Data Products



# Clock Driver Lineaerity (Range)

## Test Setup

Use the magic board.

## Software Inputs

To run the test on all channels:

[ztf@ztf-cameraN YYYYMMDD]$ archon\_tests 'driver\_linearity()'

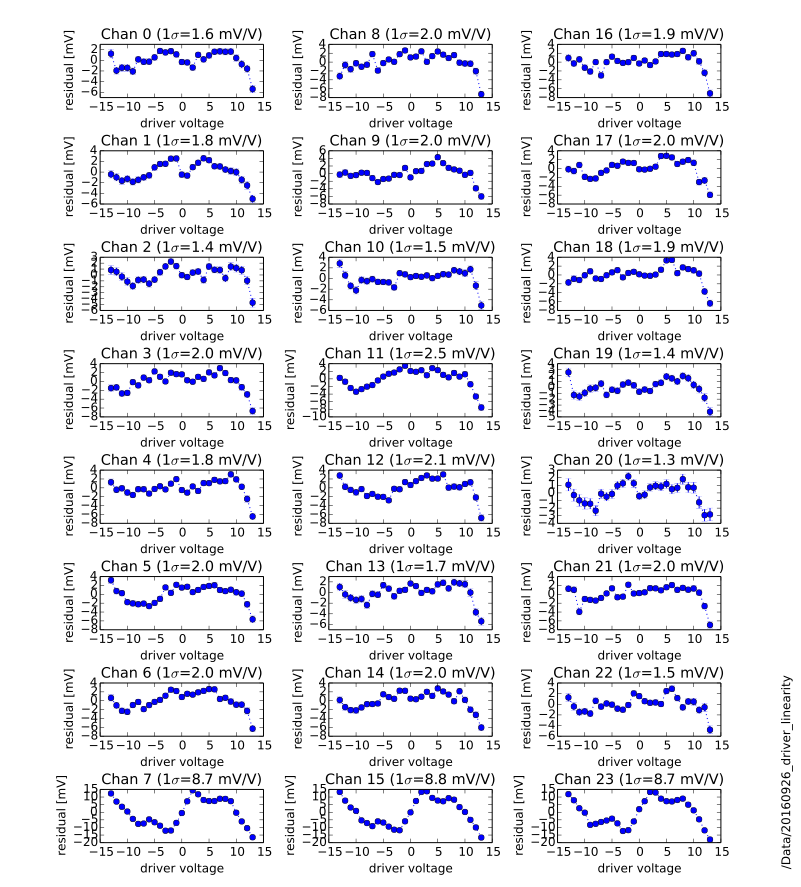
Move the files to their own directory (eg, ../YYYYMMDD\_driver\_linearity) then run the analysis script on all files (python):

>>> import PHM.driver as dd

>>> dd.linearity(savefig=True)

## Data Products

Linear fit residuals over driver range.



# Bias Noise Test

## Test Setup

Use Magic board.

## Software Inputs

To run the test on all channels:

[ztf@ztf-cameraN YYYYMMDD]$ archon\_test 'bias\_noise()'

Move the files to their own directory (eg, ../YYYYMMDD\_bias\_noise) then run the analysis script on all files (python):

>>> import PHM.noise as nn

>>> nn.plot\_bias\_noise(savefig=True)

## Data Products

# Stability Test

The Archon controller must transfer large amounts of data for long periods of time. This stability can be tested by sending known data through the controller’s ‘data pipeline’. Ideally, the controller would be able to transmit a digital pattern through the pipeline, but that capability has not been programmed into the controller. Instead, a fixed clock pattern is used to transmit a known image pattern through the whole data chain.

Two identical image patterns are subtracted and in the absence of noise, the result should be zero everywhere. The real signal has noise contributions from the clock input and the amplifier chain. The real data should have a mean of zero and a standard deviation of √2 times the clock and amplifier chain noise measured above (√2 x 4.37 DN).

## Test Setup

The test setup is similar to the clock loopback test presented in the section on the clock noise. Channel 1 of the clock card is input to channel 1 of the ADC Module. The script loaded into the Archon controller provided a fixed clock pattern which creates a striped image which is 6144x6160 pixels. There are two patterns which are transmitted through the data chain shown in Figure 8. The reason for two patterns is that the test must assure that different data is written to each buffer for every image. Otherwise, it would be unknown if fresh data was being transmitted or the same data from the previous buffer transfer.

|  |  |
| --- | --- |
| **Pattern A** | **Pattern B** |

Figure 8: Two Patterns in Stability Test

Presently, the data is saved to raw files on the ztfdev computer. To run for a long period of time, the images must be compressed to save space or must be analyzed during collection and then thrown away if there is no error. Work is proceeding on this front.

The analysis can be shown using a few frames. This analysis is from data on the ztfdev computer in the /home/ztfdev/Data/140822 directory. The fixed pattern was alternated between pattern A and pattern B. Subtracting two pattern A images yields the image shown in Figure 10.

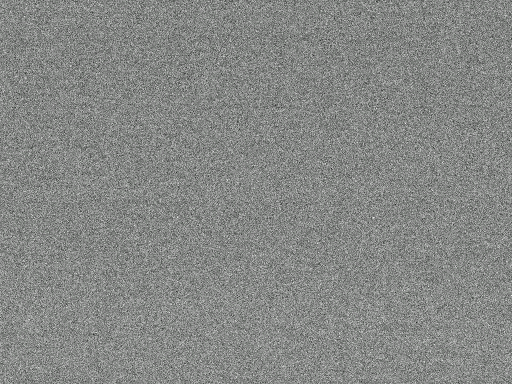


Figure 9: Pattern A Subtraction Image

A histogram of the subtracted data was platted and a Gaussian was fit to the histogram. The histogram is shown in Figure 10. The peak occurs at -0.131 DN with a standard deviation of 6.42 DN. Using the results of the input clock noise, we should see a standard deviation of 6.18 DN for the subtraction of two images.

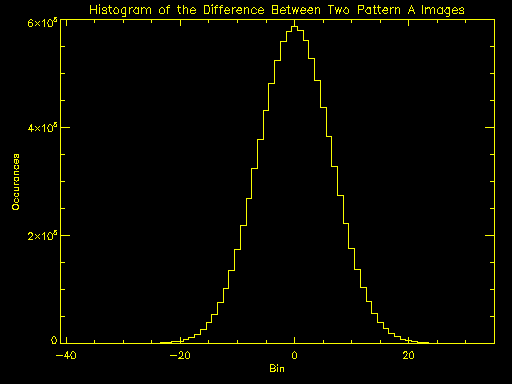


Figure 10: Histogram of the Difference Between Pattern A Images

A similar analysis can be done for the B pattern images. For the B pattern, the peak is centered at -0.148 DN with a standard deviation of 6.43 DN. A similar result to the A pattern test.

In addition to the noise of the subtracted images, the minimum and maximum values in the subtracted image should show there are no outlier values which might indicate an error in the transfer of data. For the A pattern subtraction, the minimum value is -40 and the maximum value is 34. For the B pattern subtraction, the minimum value is -34 and the maximum value is 34. With these minimum and maximum values and the noise of the subtracted signals slightly larger than expected, this is considered a successful transfer of the two images.

This method needs to be extended to data sets taken over multiple 24 hour periods.

# References

1. CCD231-C66 Data Sheet, e2v Technologies, UK

1 Bill Jasper, “Practical Telecom DAC Testing”, Test Edge Inc., pp 7-8.

2 Joey Doernberg, Hae-Seung Lee, and David A. Hodges, “Full-Speed Testing of A/D Converters”, *IEEE Journal of Solid-State Circuits* (December 1984): 820-827.

3 Application Note, “Histogram Testing Determines DNL and INL Errors”, Maxim Integrated, 18 June 2003.