# VIDEO POST PROCESSOR

The video signal from the preamp is a raw signal which must be processed and converted into digital data. In order to remove noise from the CCD’s video signal, a correlated double sample (CDS) must be done on the raw signals. In addition to the CDS, the video post processor must provide filtering before the analog to digital converter (ADC) and ensure that the common mode voltage is within the acceptable range for the ADC. The proposal for this system is to perform the CDS digitally and increase the conversion speed of the system. In addition to moving the CDS to the digital domain, we propose to have multiple samples for both the reset signal and the video signal. These multiple samples will further reduce the noise in the system.

A schematic of the proposed video post processor signal chain is shown in Figure 3.

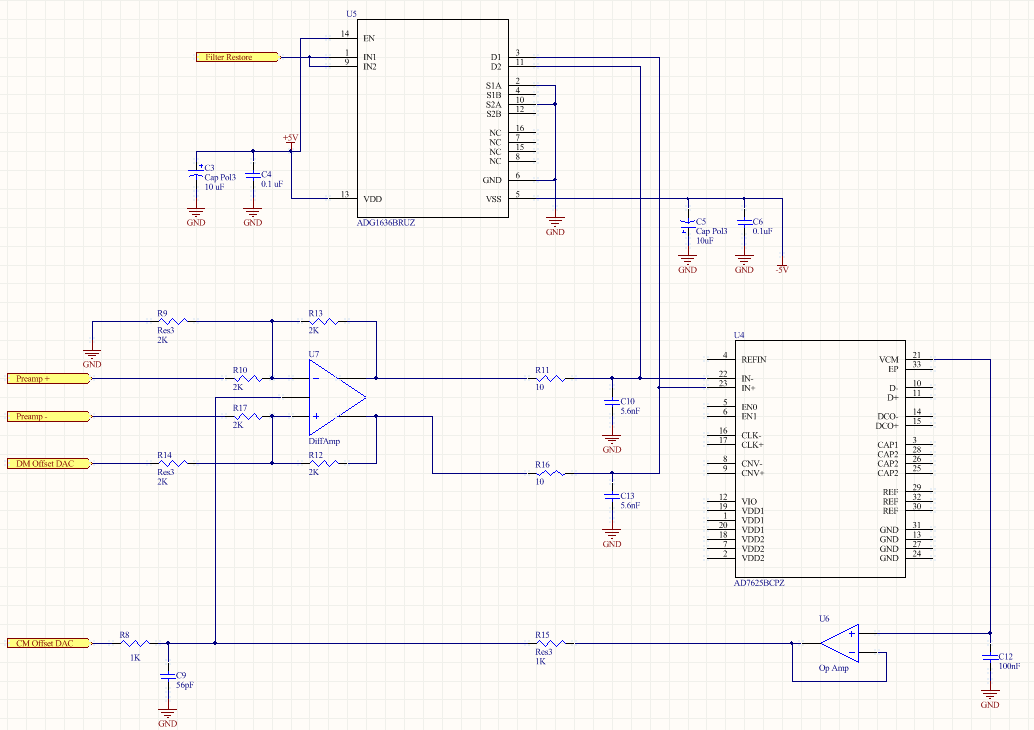


Figure 3

The design consists of a differential amplifier for the positive and negative sides of the differential signal. The output of the differential amplifier is connected to a simple one-pole RC filter which acts as an anti-aliasing filter for the ADC. The ADC is operated at a top speed of 6 MSPS. The ADC converts the CCD signal three times during reset and three times during the output signal at a maximum pixel rate of 1 MHz. The multiple conversions during each signal mode are averaged in the associated FPGA to further reduce the noise in the signal.

The common mode voltage feedback to the differential amplifier ensures that the input signal is within the acceptable common mode voltage range. According to Analog Devices, input common mode levels beyond the ADC’s range generate harmonic distortion and reduce the dynamic range of the ADC. Proper Vcm minimizes distortion and improves the bit error rate.

Note: Not shown in the present schematic is the power supply filtering and the reference voltage scheme for the ADC. The present plan is to use the internal reference voltage and power supply filter according to the data sheet of the AD7625. As the design become more mature, we will put in the remaining components for the ADC.

## ADC Buffer

The ADC buffer is an ADA4938-1 differential ADC driver3. This amplifier is designed specifically to drive the differential input of a high speed ADC. The best performance is realized when both inputs and outputs are differentially driven which makes this amplifier an ideal choice for the application.

As shown in the previous section, all of the gain in the system is in the pre-amplifier. The buffer, therefore, has unity gain. The general equation for the output differential voltage is given by the equation4:

where

and

Also, Vocm is the common mode voltage and Vip is the positive input voltage and Vin is the negative input voltage. As is the case with the above design, the equation can be simplified given that β1 = β2 = β:

As A(s) ∞, the equation further reduces to the familiar closed loop gain of

In the case of the present design, this gives the amplifier unity gain.

## Input Impedance

The signal input to the buffer is connected through a controlled impedance transmission line. The characteristic impedance of the transmission line is 100 Ω twinax. Since the connection is series terminated at the pre-amplifier driving end, no special termination must be done at the input to the buffer amplifier. Care must be taken, though, that the input impedance does not load the input signal.

Since the amplifier inputs are virtually connected, the input impedance is simply R10 + R17 which is

1 kΩ. This implies that the amplifier sees 90 % of the input signal.

## Common Mode Voltage

The VOCM pin of the ADA4938 differential amplifier sets the output common mode voltage. It is important for the proper function of the ADC for the common mode voltage of the input signal to be within ± 50 mV of Vref/2. The ADC provides a common mode output which is half of the reference voltage of the ADC. This output from the ADC is buffered to drive the output common mode voltage pin of the amplifier.

## Output Offset

The offset in the input differential signal must be controlled to keep the signal within the ADC range and to adjust for ADC offset errors. This offset signal needs to be a differential signal and will be injected into the positive side of the signal through a 2 kΩ resistor. A 2 kΩ resistor is added to the negative input to keep the balance of the amplifier.

The circuit can be analyzed by using the fact that there are two feedback loops for the amplifier and the difference in voltage at the positive and negative input pins is zero. Using these facts and analyzing the current flow through the resistors, the output differential mode voltage is

The voltage from the DAC directly adds to the differential output voltage. The voltage range and resolution of the DAC is yet to be determined.

## Anti-Aliasing Filter

The anti-aliasing filter attenuates higher frequency signals from entering the ADC. For this application a simple one-pole RC filter is used. The sample frequency of the ADC is 6 MHz, so to filter out any aliasing signals; the corner frequency of the filter is set to 3 MHz. A 10 Ω resistor with a 5.6 nF capacitor to ground forms the filter. The resistor isolates the amplifier from the capacitive load, and the capacitor to ground provides a charge reservoir for the input to the ADC. The two sides must be well matched for good CMRR and so high precision resistors and capacitors are used.

Since the 3 dβ frequency of the filter is at the Nyquist frequency of the ADC, memory effects will occur in the filter’s capacitor. To clear the temporal smear from this aggressive filter, a reset switch is included in the design. This analog switch to ground is an ADG1636 and has a maximum leakage current of 2 nA over the desired temperature range. As shown in the preamplifier section of this note, the poisson noise current is 25 fA/√Hz. This current noise over the 10 Ω amplifier isolating resistor gives a 0.25 pV/√Hz noise signal to the ADC. This contribution to the noise is negligible and can be ignored.

The on resistance of the switch to ground must be low enough to discharge the capacitor within the time of a single pixel. For the present switch, the maximum on resistance is 1.4 Ω. With a 5.6 nF capacitor, the time constant is 7.84 nF. A turn on time of 166 ns could reduce the on time of the switch to about 834 ns. The worst case on time is still over 100 time constants and should be sufficient to remove the charge from the anti-aliasing filter capacitor.

When the anti-aliasing filter is being discharged, the differential op-amp sees a 20 Ω differential load. This is an acceptable load for the ADA4938-1. For the ADC, the inputs are directly tied to ground and the input common mode voltage of VREF/2 ± 50 mV is violated. This can cause distortion in the amplifier and a recovery time is under investigation.

## ADC

The selected ADC is an Analog Devices AD7625. This ADC has a maximum sample rate of 6 MHz and a 16 bit resolution with no missing codes. In this design, the internal reference is used. This internal reference sets the input differential voltage range at ±4.096 V. A mid-range voltage of 0 V has an output code of 0x0. The remaining codes in the voltage range are in twos complement format (i.e. positive full scale is 0x1FFF and negative full scale is 0x1000). A single bit is 62.5 µV.

The sample rate for the application will be pushed to its maximum of 6 MHz. This sample rate allows for three samples of the reset signal and three samples of the charge signal. The oversampling of each part of the CCD signal helps to reduce the noise in the signal by averaging the samples. Since both the reset and charge signals are digitized, the correlated double sampling (CDS) now occurs in the digital realm. The subtraction of the averages from each part of the CCD signal will be the ultimate data output from the data FPGA. The minimum time between conversions for the ADC is 166 ns which translates to a maximum sampling frequency of 6.02 MHz.

The CMRR of the ADC is 60 dβ for a 1 MHz signal applied to both VIN+ and VIN- inputs refers to the power of the full frequency spectrum to the power of an 80 mV applied sine wave of 1 MHz.

The differential non-linearity of the ADC is ±0.3 LSB. This DNL guarantees no missing codes. The integral non-linearity is ±0.45 LSB. The low INL means the ADC is a very linear device and deviates less than an LSB over the full scale range.

## Signal Processing -- Digital Integration and CDS

Moving the CDS to the digital realm requires some type of processor or FPGA to handle and process the extra data. A Complex Programmable Logic Device (CPLD) is a good choice to handle this level of processing. A lower complexity FPGA would also be suitable. This post processor must be able to receive data at a 6 MHz rate, average the reset and signal samples, and perform the CDS.

Averaging of the signals can help to improve the noise performance of the system. Averaging is analogous to inserting a low pass filter into the circuit where the time constant is given by

𝜏 = N/Fs where N is the number of samples and Fs is the sampling frequency. In this case, a 2MHz low pass filter is realized by the post-processing. This gain is realized only when the samples are independent from one and other.

Another technique for increasing the resolution of the ADC is by oversampling and using decimation to increase the resolution of the ADC by 1 bit. This requires at least 4x oversampling which cannot be done at the maximum desired pixel frequency with the present ADC. This mode may be a useful option for slower readout speeds, but this project will not focus on this mode due to the need for very fast readouts.

It should be noted that the above two techniques will not calculate correct data at the limits of the ADC range. That is, when the signal is near -4.096 V or +4.096 V, any noise which causes the signal to be outside the voltage range will be converted into the minimum or maximum code. This will create an incorrect average due to clipping of the signal. Any signals near the limit must be dealt with differently.

After the signals are averaged, the CDS is performed by subtracting the reset signal from the charge signal. The resulting data can either be stored in the data FPGA or transmitted to the digital card or a “master” card for storage. This detail must be studied further to determine the best place for data storage before it is transmitted to the host computer. For controllers connected to multiple CCDs, the order of data transmission must be determined. The controller must also allow for a CCD data stream to be disabled and removed from the overall data stream.

## Output Noise Analysis

A systematic review of the noise sources can provide a basis for the calculation of the total noise from the ADC buffer. The noise sources are from the amplifier itself in terms of input voltage noise, input current noise, and common mode voltage noise. The surrounding components also contribute to the noise, i.e. the feedback resistors and gain resistors. A model of the noise sources is shown in Figure 4.

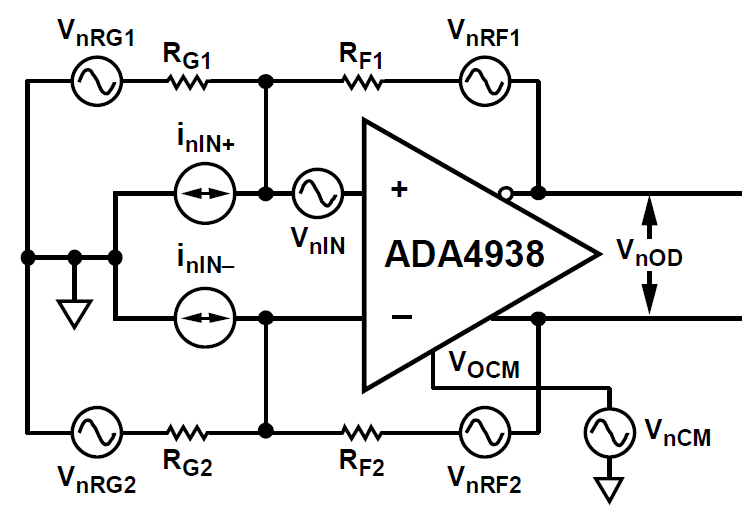


Figure 4

The input voltage noise (VnIN), input current noise (InIN+ and InIN-), and common mode voltage noise (VnCM) are all properties intrinsic to the differential amplifier. The value of these sources of noise can be found in the ADA4938 data sheet and are entered in Table 2.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Input Voltage Density (nV/√Hz) | Output Multiplication Factor | Output Voltage Density (nV/√Hz) |
| Differential Input | 2.6 | GN | 5.2 |
| Inverting Input | 4.8 | GN | 9.6 |
| Noninverting Input | 4.8 | GN | 9.6 |
| Vocm Input | 7.5 | GN(β1 – β2) | 0 |
| Gain Resistor R10 | 5.74 | GN(1 – β1) | 5.74 |
| Gain Resistor R17 | 5.74 | GN(1 – β2) | 5.74 |
| Feedback Resistor R13 | 5.74 | 1 | 5.74 |
| Feedback Resistor R12 | 5.74 | 1 | 5.74 |

Table 2

The total output voltage density from the ADC buffer is the square root of the sum of squares of all of the contributions.

For completeness, the single pole RC filter after the buffer amplifier must also be considered in the noise calculation. Specifically, the two resistors (R11 and R16) contribute thermal noise to the input of the ADC.

This level of contribution is small compared to the buffer amplifier and its components and can be safely ignored.

Using a bandwidth of 1.5 MHz, we have a total noise of for the ADC buffer amplifier.

The anti-aliasing filter and the reset switch for the filter contribute kTC noise to the input signal of the ADC. This noise is due to the fluctuation of the remaining charge on the capacitor after it is reset and is directly related to the capacitor value. The formula for the reset noise is given by

Where k is Boltzmann’s constant, T is the temperature, and C is the value of the capacitor. In addition to reset noise, the RC filter contributes a voltage noise given by the formula

For the 5.6 nF capacitor, the kTC voltage noise is 0.86 µV and is uncorrelated for the two input filters. Even though this increases the noise contribution to the ADC to 1.22 µV, the voltage noise input to the ADC is negligible due to the RC filter.

The kTC reset noise for the filter is 30,000 e-. This reset noise translates to a voltage reset noise of 0.14 µV. Again, this reset noise is uncorrelated between the two filters which increases the reset noise input to the ADC to 0.20 µV and is a negligible contribution to the input noise to the ADC.