Digital Correlated Double Sampling for ZTF

Roger Smith and Stephen Kaye

California Institute of Technology

**Abstract**

We review the design of the Digital Correlated Double Sampler for the Zwicky Transient Facility’s 64 channel readout and show how it increases the dynamic range beyond 16 bits to handle the >300ke- full well, while comfortably oversampling the read noise. The effects of the AD converter quantization and DNL will be examined, leading to choices of gain and antialiasing frequency, which are independent of pixel rate. We show that a 2 pole antialiasing filter allows digital CDS to achieve similar noise performance to dual slope integration with only 10 samples per pixel. This allows a moderate speed 16 bit ADC with excellent performance to be used. Output resolution exceeds the 16 bit ADC resolution, but rather than adopt a non-standard numeric format, word width is extended to signed 32 bit integers, then lossless (Rice) compression is applied prior to writing to disk for the first time.

# Introduction

Impressive advances in the speed and precision of compact, low power Analog to Digital converters, and in the speed and complexity of Field Programmable Gate Arrays, have enabled correlated double sampling (CDS) to be performed in the digital domain with simple, compact circuitry. We will explain why we expect this approach to deliver superior performance in the Zwicky Transient Facility, compared to either conventional clamp-sample or dual slope integrators.

Digital CDS (DCDS) has already been used successfully in other high channel count CCD mosaics which read out at moderately high speed such as the STARGRASP controller for Pan-STARRS[1], the Reflex and Archon controllers sold by Semiconductor Technology Associates[2] and the CCD controllers used by e2v in the JPAS camera[3]. To assist others who may be contemplating a similar path, we present a design study for the DCDS scheme to be implemented for the 64 ZTF science channels operating at 1 megapixel per second. In particular, we examine the impact of adopting only modest oversampling rates, using 10 MHz ADCs. The modest conversion rate allows 16 bit ADCs with excellent differential non-linearity and low input noise be used. These have low cost and low power in a compact package, as needed in high channel count systems.

We will argue that DCDS also has a place in slower readout applications that demand the lowest possible noise. We plan to test this hypothesis in the four guide/focus CCDs for ZTF. (Guiders need high frame rate but pixel times can be long since parallel shifts dominate read time for Region-of-Interest readout.)

# Digital Correlated Double Sampling - The Idea

DCDS is nothing but dual slope integration in the digital domain, but we will show that it has some subtle advantages. Signal theory tells us that a time domain signal can be fully described by a series of uniformly spaced samples at or above twice the highest frequency in the signal. In our design[4], Figure 1, differential CCD outputs are amplified close to the CCD, then transmitted differentially to an AD8139 ADC driver that removes the common mode component and supplies a purely differential signal to the 10 MHz 16 bit AD converter (AD7626).

An anti-aliasing filter with two pole roll off and corner frequency at 5 MHz is placed just before the AD converter. Low inductance capacitors (several in parallel) provide the low output impedance at high frequencies required by the ADC. This filter attenuates frequencies above the Nyquist limit, which would show up in the passband at beat frequencies (“aliases”) that are the difference between the sample rate and the true frequency.



Figure 1: *Full Signal Chain Schematic*

AD conversion occurs continuously at maximum speed, transmitting serial data and clock as 160 MHz LVDS signals to the adjacent Field Programmable Gate Array (FPGA). To emulate dual slope integration, the FPGA initializes a 32 bit accumulator to zero, converts the serial data stream to 16 bit words, then simply subtracts post-reset samples and adds samples after the charge dump.

# Data Handling

We plan to operate each four-channel CCD in ZTF with a single board controller communicating with the host via one USB2 link. This locates the ground star point optimally, *inside the board*, allowing clock, digital and video grounds to be joined *at the ADC* without traversing connectors and long wiring paths. Locating the FPGA right next to the ADCs keeps their high-speed serial outputs very short. USB links from four single board controllers will be combined into one optical fiber in a separate commercial USB extender. Four fibers serve the 16 CCD focal plane. Another serves the guide and focus CCDs. (See Figure 2.)

USB2 supports up to 400mb/s. The host processor may not be able to support this full rate concurrently on four links at once, however only 128 mb/s is required to support 32 bit unsigned data on four channels at 1 MHz pixel rate.

The 32 bit accumulator provides more numeric precision than needed but adopting signed 32 bit integer format eliminates the need to “unpack” a custom numeric format. We plan to convert the 32 bit unsigned data to FITS Tile Compression[4] format prior to the first disk write. Tile Compression leaves headers uncompressed so they can be interrogated efficiently. One compressed FITS file will be stored per CCD, with files being distributed among multiple host computers. Files are transmitted over a microwave link from Palomar Mountain, ultimately arriving at the IPAC data center without ever being merged into a file-per-exposure.



Figure 2: *ZTF System Diagram.*

With Digital CDS the number of bits needed in the accumulator grows faster than the S/N. To improve data compression without loss of information, one could normalize to discard excess low order bits containing only noise, but for small numbers of samples per pixel this data compression improvement will be minor.

# Advantages of Digital CDS – an overview

## Simplicity and compactness

The analog signal path has been reduced to its simplest form: AC coupler, preamplifier with modest gain, ADC buffer, band limiting filter and ADC. The digital processing is well within the capabilities of mainstream FPGA’s which are likely to be included on the board to provide the communications interface. FPGA resources are generally sufficient to support several channels in one device. The serial interface to the ADC requires minimal pin count and by placing several accumulators in one FPGA their outputs can be multiplexed onto a common communication path.

## Wide frequency range

DCDS has a high bandwidth path from CCD to ADC and can thus operate at higher than normal pixel rates, down to two samples per pixel. Usually the pixel rate will be limited by the serial clock drivers rather than the corner frequency of the anti-aliasing filter.

Digital CDS can run slower without any adjustment to gain or bandwidth. One simply averages more samples. Contrast this to clamp-sample where component tuning is needed to change filter bandwidth or dual slope where analog gain has to be reduced to compensate for an increase in integrator gain at long integration times.

## Excellent low frequency rejection without tuning

The low frequency rejection of analog CDS is dependent on component tolerances and/or tuning and, even when carefully tuned, is typically limited to about one part in a few thousand by capacitor non-linearity. Digital CDS uses the same signal path and polarity for all samples and thus requires no tuning and achieves better low frequency rejection.

## High dynamic range, exceeding that of 16 bit ADC

This topic will be discussed in more detail in section 5. The gain is set so that a 16 bit ADC optimally samples the noise for single samples. As samples are combined the numerical resolution increases beyond the dynamic range of the 16 bit converter. If the pixel rate is reduced, more samples are averaged reducing the noise without changing the maximum signal that can be handled. This increase in dynamic range occurs naturally as larger numbers are produced by coadding. No changes in hardware or processing parameters are needed.

## True zero

A minor feature of DCDS is that the artificial offset to support unipolar ADC operation is hidden from the user, since this offset occurs before the differencing of samples. Any offset from zero seen in the overscan or bias frames is thus diagnostic of electronic effects such as clock feedthrough instead of being dominated by the applied output offset. Negative data values can be produced by noise and are supported by the *signed* integer format. Contrast this to analog CDS where the input offset to the ADC (added to avoid underflow of the unipolar ADC) is seen in the data and masks the true offsets.

## Digital Oscilloscope Modes

Direct monitoring of the waveform from the CCD can be provided by simply disabling the differential averaging process and transmitting raw data instead. Usually this would only be done for one video channel at a time to avoid exceeding the communication bandwidth to the host.

For diagnostics, one is often interested in the details of the waveform for dark pixels. Since this should not vary from pixel to pixel except for noise, it is possible to operate in “sampling oscilloscope” mode, delaying the samples to interpolate. For example, we have a 10 MHz sample rate but 100 MHz timing resolution and can thus apply 10 different phase delays. The usefulness of this mode will depend on the choice of the anti-aliasing filter’s corner frequency. The more aggressive filter will produce more sample-to-sample correlation so that phase shifting will add little new information. A further complication is that each pixel’s samples will probably need to have the mean of the post-reset samples subtracted to suppress kTC noise.

# Gain

It is desirable that for raw samples when only CCD read noise is present, noise should be 2 to 3 ADU rms to assure that ADC Differential Non-Linearity (DNL), ADC noise and quantization produce negligible errors when the samples are averaged.

DNL is a variation in the magnitude of the voltage change corresponding to one output code. When samples are distributed over many codes then averaged, this error is smoothed. DNL errors typically alternate sign for successive AD output values so only a few ADU of noise is required to provide adequate smoothing. When multiple images are combined, shot noise will provide further smoothing. DCDS provides this smoothing even in single images.

Given a typical 3 e- read noise floor (slow scan) the 3 ADU noise rule implies 1 e-/ADU conversion gain. If the same CCD has 300,000 e- full well one needs a unipolar ADC to have 18 bit dynamic range. In ZTF, the read noise at 1MHz for differential inputs is 7e- (typical), so only 17 bit dynamic range is needed. 18 bit converters are available but we believe the Digital CDS approach is more forgiving and has the additional advantages listed above.

For Digital CDS using a 10 MHz sample rate, the anti aliasing filter corner frequency is set to ~5MHz. The equivalent noise bandwidth for dual slope integration is the pixel frequency, if sample time is half the pixel time. The typical noise curve given in the CCD231-C6 data sheet[6] predicts 10 e- noise for clamp-sample at 5 megapixels per second for conventional single sided CCD output. This would scale to 14 e- for differential, so noise equaling 3 ADU will be produced with conversion gain set to 14/3 = 4.7 e-/ADU. A 16 bit ADC then saturates at 306ke-, and thus can digitize both the full well and the per-sample noise.

The read noise stated in the data sheet may prove to be somewhat optimistic and electronic noise has yet to be added so higher conversion gain and thus more signal headroom may become available. If a bit more headroom is required the 3 ADU noise rule can also be relaxed slightly. Moving in the other direction, the CCD output is *linear* for only 200,000 e- so lower conversion gain (higher electrical gain and more noise in ADU) will be possible if it proves unnecessary to digitize the non-linear part of the signal range for crosstalk correction. This would be unusual, but is a possibility given the use of differential CCD outputs.

# Noise

Gach[7]has reported a noise advantage when heavier weighting is given to the samples close to the charge dump (either side), but this has not been reproduced by Clapp[8]. Our expectation is that the noise at 1MHz will be predominantly white so that the best strategy will be to give equal weighting to all samples.

We have selected the AD7626 16 bit converter, which supports 10 MHz conversion rate. The “charge redistribution successive approximation” architecture of the AD7626 delivers low noise (<0.5 ADU), excellent DNL (+-0.35 ADU), with low power (136mW) in a very compact (LFCSP) package. LVDS serial output makes interfacing of multiple ADCs to one FPGA easy since the pin count is low. The conversion rate is high enough to support the oversampling needed for DCDS while being low enough that the bit rate (222Mhz) can be supported by FPGAs such as the Virtex 5 planned.

The primary DCDS design decisions are the selection of ADC sample rate and anti-aliasing filter bandwidth. Let’s examine the impact of these choices. Setting the corner frequency of an anti-aliasing filter with one pole roll-off to 5 MHz (half the AD conversion rate) results in 96% settling of the reset feedthrough or charge dump edges in one AD conversion time. With four or five conversions per half pixel time, there will be no problem with gain loss due to inadequate settling, and there is some latitude for more aggressive analog filtering to reduce the aliasing of noise power above Nyquist frequency due to the finite slope of the aliasing filter cutoff. The design in Figure 1 has a single pole roll off in the preamplifier (due to C3 and C4) and another single pole roll off at the input of the ADC due to C5 and C6. The possibility of an additional pole of roll off exists by converting this filter from simple RC to a critically damped LRC filter, however the effect on the ADC has yet to be studied. In all cases very low inductance capacitors and wiring are needed to assure optimum ADC performance.

# What Sample Rate?

We seek to optimize for compactness, cost and performance (DNL and noise) by selecting the *slowest* ADC. How many samples per integration are sufficient to reach the same noise performance as the analog dual slope integrator? The rms output noise,may be found by summing the output noise power over all frequencies:

 (1)

where

 electronic transfer function magnitude, including antialiasing filter

If noise is white, (1) can be written

 (2)

For analog CDS the corner frequency of the anti-aliasing filter is placed well above the dual slope integrator passband so a good approximation is:

 (3)

For the dual slope integrator, transfer function squared is given by

 (4)

We will see below that the transfer function for the digital differential averager closely resembles the dual slope integrator only at low frequencies, and requires an antialiasing filter to suppress high frequencies that would alias into the passband. Higher sample rates push these aliases to higher frequencies where they are more easily filtered, but at some penalty in ADC performance, power dissipation, size and cost. We will show that only moderate sample rate is required (thus a better ADC), if a steeper (but inexpensive) antialiasing filter is used.

# Transfer Function for Digital CDS

The total noise after subtracting 4 samples after reset from 4 samples after charge dump (8 total samples per pixel), without normalization, is:

  (5)

Invoking the Fourier translation theorem, which states that

if

then ,

and linear superposition, (5) becomes:

 (6)

The “transfer function” is defined as:

For any complex number, the magnitude squared is the product of the number and its complex conjugate. Thus,

Applying the distributive law, then collecting terms, we simplify by noting that

 and

so for 8 samples per pixel,

Results for up to 14 samples per pixel are shown in Table 1. Note that all terms are cosines and thus approach one as the argument approaches zero, yet we know that CDS response tends to zero at low frequencies. This requires that coefficients (i.e. columns in Table 1) must sum to zero.

# Results

Figure 3 shows how, as expected, the aliased power moves to higher frequencies as the number of samples per pixel increases. The important observation is that only four or five samples need to be averaged to produce a transfer function, which closely approximates the dual slope integrator, below Nyquist.

Table 1: Transfer function squared can be constructed for n samples per pixel by summing the terms at left, after scaling by coefficients in the relevant column, then normalizing by n2

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Samples/pixel🡪** | **2** | **4** | **6** | **8** | **10** | **12** | **14** |
| 1 | 2 | 4 | 6 | 8 | 10 | 12 | 14 |
| cos( | -2 | 2 | 6 | 10 | 14 | 18 | 22 |
| cos( |  | -4 | 0 | 4 | 8 | 12 | 16 |
| cos( |  | -2 | -6 | -2 | 2 | 6 | 10 |
| cos( |  |  | -4 | -8 | -4 | 0 | 4 |
| cos( |  |  | -2 | -6 | -10 | -6 | -2 |
| cos( |  |  |  | -4 | -8 | -12 | -8 |
| cos() |  |  |  | -2 | -6 | -10 | -14 |
| cos( |  |  |  |  | -4 | -8 | -12 |
| cos( |  |  |  |  | -2 | -6 | -10 |
| cos( |  |  |  |  |  | -4 | -8 |
| cos( |  |  |  |  |  | -2 | -6 |
| cos( |  |  |  |  |  |  | -4 |
| cos( |  |  |  |  |  |  | -2 |

Since a perfectly sharp antialiasing filter cannot be built, we examine the trade between filter complexity (steeper slope) and the sample rate required (which comes at some penalty in ADC metrics).

Figure 4 shows the transfer function for differential averaging with a one pole anti-aliasing filter and 4 MHz corner frequency. There is still significant noise power in the aliases until sample rate becomes significantly higher than the 10MHz provided by the AD7626 converter. See Table 2. However, Figure 5 shows that with a still-simple 2 pole filter, the power in aliases is small even for 4 samples per average and almost negligible for 5 samples. Assuming 2 samples are lost to pixel overheads such as CCD reset then this corresponds to 830 kHz and 1 MHz pixel rates respectively.

Up to this point we have neglected the normalization step. A careful reading of papers on this subject reveals that discrepancies in the normalization factors are common. We have therefore crosschecked our analytical derivation of the transfer function with a direct numerical analysis in which the differential averaging was performed on a long sequence of sinusoidally varying values with unit peak-to-peak amplitude. Peak to peak amplitude of the resulting sine wave was plotted versus frequency to validate the analytical solutions both for shape and normalization. We find that normalizing by number of samples per pixel squared produces good agreement with the normalization adopted in equation (4).



Figure 3: Transfer functions for analog dual slope compared with digital differential averaging at different sample rates (same total integration time).



Figure 4: Same as Figure 3 but with 1 pole filter at 4MHz corner frequency. There is still significant noise power at frequencies above Nyquist.

Figure 5: Same as Figure 3 but with 2 pole filter at 4MHz corner frequency. Aliased power is minimal so that noise is almost identical to dual slope integration for 5+5 samples.

# Conclusions

Table 2 shows the square root of integrated noise *power* for DCDS divided by that for dual slope integration in the case where CCD noise dominates and is white at frequencies above the pixel rate where the transfer functions may differ. At moderate sample rates, 8 to 10 samples per pixel, the dual slope integrator remains superior. However Table 2 shows that a simple filter with 2 pole roll off is sufficient to almost eliminate this difference. We conclude that this is more cost effective than using a higher speed AD converter to push the aliased frequencies further from the filter corner. By choosing only 10 MHz conversion rate for 1 MHz readout of ZTF, we are able to utilize the AD 7626 16 bit converter which offers an excellent combination of compactness, low power, resolution, low input noise good DNL and affordability.

Table 2: Percentage increase in CCD read noise for DCDS compared to dual slope, with various samples per pixel (anti-aliasing filters fc=4Mhz).

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Samples 🡪 | 4+4 | 5+5 | 6+6 | 7+7 |
| 1 pole filter | 21% | 12% | 6.3% | 3.4% |
| 2 pole filter | 7.2% | 2.0% | -0.5% | -1% |

A remaining design choice is the selection of either a critically damped LRC antialiasing filter at the input of the AD converter, or sequential single pole filters at the differential preamp and the AD converter input, as shown in Figure 1.

# References

1. P.Onaka, et al., “GPC1 and GPC2: the Pan-STARRS 1.4 gigapixel mosaic focal plane CCD cameras with an on-sky on-CCD tip-tilt image compensation”, SPIE vol. 8453, 2012.
2. R. Bredthauer, K. Boggs, G. Bredthauer, “STA CCD Detector, Controller and System Developments” Scientific Detector Workshop 2013, Astrophysics and Space Science Library (these proceedings), 2013.
3. P.R. Jorden, et al., “A gigapixel commercially manufactured cryogenic camera for the J-PAS 2.5m survey telescope” SPIE Vol. 8453, 2012.
4. R.Smith, S.Kaye, "Fully Differential Signal Path for the ZTF Mosaic" Scientific Detector Workshop 2013, Astrophysics and Space Science Library (these proceedings), 2013.
5. W. Pence, R. Seaman, R. White “Lossless Astronomical Image Compression and the Effects of Noise” <http://arxiv.org/pdf/0903.2140.pdf>, 2009.
6. e2v Technologies, CCD231-C6 data sheet, <http://www.e2v.com/products-and-services/high-performance-imaging-solutions/> (2013)
7. J-L. Gach, D. Darson, C, Guillanume, M. Goillandeau, C. Cavadore, P. Balard, O. Boissin, J. Boulesteix, “A New Digital CCD Readout Technique for Ultra-Low-Noise CCDs” Publications of the Astronomical Society of the Pacific, Vol. 115. pp. 1068-1071, 2003
8. M.J. Clapp, “Development of a test system for the characterization of DCDS CCD readout techniques” SPIE Vol. 8453, 2012
9. J. Janesick, *Scientific Charge Coupled Devices*, SPIE press, ISBN 0-8194-3698-4, pp. 578-579